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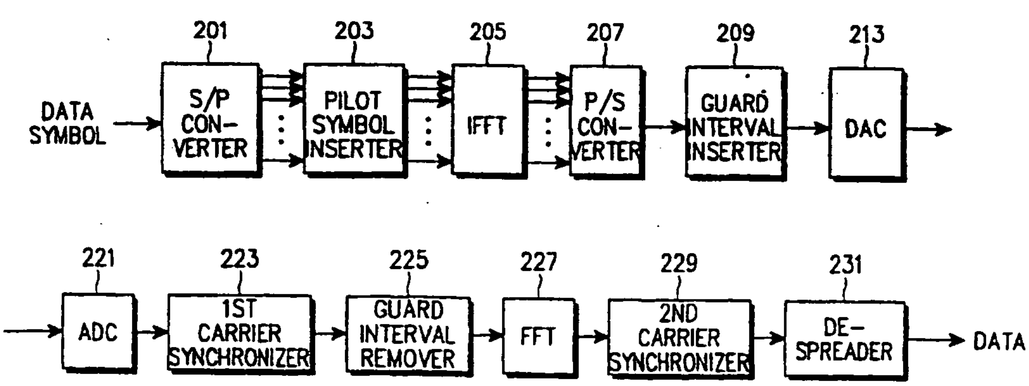

(57) Abstract: An apparatus of compensating for a frequency offset using a guard interval and a pilot symbol, which are inserted at a transmitter, in an OFDM (Orthogonal Frequency Division Multiplexing) system. The OFDM system receives an OFDM signal in which a pilot symbol is inserted in data of a frame unit at regular intervals and a guard interval is inserted in a data symbol. In the system, a first carrier synchronizer receives a data symbol stream obtained by converting the OFDM signal to digital data, and detects a guard interval of each data symbol, to compensate for a coarse frequency offset. A fast Fourier transform part OFDM-demodulates a signal output from the first carrier synchronizer. A second carrier synchronizer detects the pilot symbol from the demodulated data symbol stream to compensate for a fine frequency error.

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APPARATUS OF COMPENSATING FOR FREQUENCY OFFSET USING PILOT SYMBOL IN AN ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a frequency offset compensation apparatus for an OFDM/CDMA (Orthogonal Frequency Division Multiplexing/Code Division Multiple Access) system, and in particular, to a frequency offset compensation apparatus which compensates for a frequency offset (or frequency error) using a guard interval and a pilot symbol.

2. Description of the Related Art

As the types of the recent multimedia services are diversified, it is necessary to transmit data at high speed. In addition, as the user's demand for construction of a wireless network increases, a wireless asynchronous transmission mode (hereinafter, referred to as "WATM") market is expanded. Thus, every country forms various organizations for WATM standardization to expedite implementation of the WATM technology. For implementation of such a high-speed data transmission technology, active researches are being carried out on a method for using the orthogonal frequency division multiplexing (hereinafter, referred to as "OFDM") technology in implementing the high-speed data transmission. In the OFDM technology, data is transmitted on a plurality of subcarriers after inverse fast Fourier transform (IFFT), and the transmitted subcarriers are converted to the original data in an OFDM receiver through fast Fourier transform (FFT).

FIG. 1 illustrates a structure of a general OFDM/CDMA system. With reference to FIG. 1, a description will be made of the structure and operation of a transceiver in the OFDM/CDMA system.

First, the structure of a transmitter will be described. A spreader 101 spreads data symbol streams to be transmitted by multiplying the data symbol streams by a code of an N rate in a data symbol unit. Herein, N data bits obtained by multiplying the data symbol by the code of N rate will be referred to as "data samples". The N data samples spread from the data symbol are parallelized by a serial-to-parallel (S/P) converter 103

and then, input to a pilot sample inserter 105. The pilot sample inserter 105 receives the N data samples in parallel, punctures the received data samples at regular intervals, and then inserts pilot data samples as shown in FIG. 2, and the pilot sample-inserted data symbol is provided to an inverse fast Fourier transform (IFFT) section 107. The IFFT 107 receives in parallel the pilot sample-inserted data samples in the data symbol unit and performs inverse fast Fourier transform on the received data samples. In the following description, the IFFT-transformed data output from the IFFT 107 will be referred to as "OFDM symbol". The OFDM symbol is also comprised of N data samples. The OFDM symbol output from the IFFT 107 is input to a guard interval inserter 109. The guard interval inserter 109 copies a part of the rear end of the received OFDM symbol and inserts it in the front of the OFDM symbol. The guard interval-inserted OFDM symbol is converted to an analog OFDM symbol by a digital-to-analog converter (DAC) 111 and the converted analog OFDM symbol is transmitted after up-conversion.

Next, a receiver down-converts the analog signal transmitted from the transmitter. Because of the inaccuracy of an oscillator used during the down-conversion, the baseband signal includes a frequency offset. The analog signal is converted to a digital OFDM symbol by an analog-to-digital converter (ADC) 121 and then, applied to a guard interval remover 123. The guard interval remover 123 frame-synchronizes the OFDM symbol output from the ADC 121, and after frame synchronization, removes the guard interval included in the OFDM symbol, the guard interval-removed OFDM symbol being applied to a fast Fourier transform (FFT) section 125. The FFT 125 FFT-transforms the OFDM symbol output from the guard interval remover 123 and outputs a data symbol. At this point, since a signal is obtained which is shifted by the frequency offset included during the down-conversion, it is difficult to recover the original data. Particularly, in an OFDM/CDMA system where a desired signal is carried at each frequency band, the frequency offset should be correctly estimated and compensated for to recover the original signal. To compensate for the frequency offset, a carrier synchronizer 127 detects a pilot sample from the data symbol output from the FFT 125, and performs carrier synchronization using the detected pilot sample. A despreader 129 despreads the data symbol output from the FFT 125, which was spread into N data samples, and outputs the original data symbol.

The FFT 125 generally recovers the frequency offset using the FFT characteristics shown in Equation (1) below.

$$X[n]W_N^{K_0 n} \leftrightarrow X[k-k_0](W_N = e^{\frac{-j2\pi}{N}}) \quad \ldots\ldots (1)$$

where X[n] is an input signal in a time domain, which is input to the FFT, $W_N^{K_0 n}$ is an offset term, and $X[k-k_0]$ denotes a received signal with a frequency offset, which is shifted by k_0 from the transmission signal during down-conversion.

FIG. 2 illustrates a data structure used in the general OFDM/CDMA system, which shows that the pilot data samples are inserted after puncturing N data samples for each data symbol in a specific pattern. Since the pilot data samples are inserted in a specific pattern, Equation (1) is calculated using the pilot data samples and the frequency offset is compensated for by calculating a shift amount k_0 of the data calculated by Equation (1).

In an ideal system, since the pilot samples received as shown in Equation (1) are received in a position shifted by k_0 samples from the original reference sample position, it is possible to calculate the frequency offset k_0 by estimating the shifted value using a correlator. However, in the OFDM/CDMA system, use of the above pilot samples causes such performance degradation as an increase of over 2 times in a data rate, complication of a receiving stage for compensating for the frequency offset, and an increase in a noise level, so that it is difficult to use the pilot samples.

A non-ideal system has the more serious problems. The factors affecting the IFFT-transformed signal include a timing error, a common phase error (CPE) and the noises. In the receiver, a timing error n_ε in a time domain, after passing the FFT stage, are expressed by the product of the original signal in the frequency domain and an exponential term. This ultimately affects even the pilot sample value, so that an increase of this value may cause considerable performance degradation of the correlator. Therefore, in the OFDM/CDMA system, it is difficult for the conventional frequency offset compensation method to detect a correct frequency offset value.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a transmitter which inserts pilots (or pilot symbols) of a symbol unit at regular intervals when transmitting a

data symbol steam, to enable exact frequency offset correction at a receiver.

It is another object of the present invention to provide a frequency offset compensation apparatus which compensates twice for a frequency offset using a guard interval and a pilot symbol included in received frame data in which pilot symbols are inserted at regular intervals.

To achieve the above object, a transmitter for an OFDM system includes a modulator for OFDM-modulating a received data symbol, a guard interval inserter for inserting a guard interval in the OFDM-modulated data symbol, a pilot symbol inserter for inserting a pilot symbol in the data of frame unit output from the guard interval inserter at regular intervals, and an analog-to-digital converter for converting the data output from the pilot symbol inserter to an analog signal.

To achieve another object, a receiver for an OFDM system, which receives an OFDM signal for which a pilot symbol is inserted in data of a frame unit at regular intervals and a guard interval is inserted in a data symbol, includes a first carrier synchronizer for receiving a data symbol stream obtained by converting the OFDM signal to digital data and compensating for an approximate frequency offset by detecting the guard interval of each data symbol, a fast Fourier transform section for OFDM-demodulating the signal output from the first carrier synchronizer, and a second carrier synchronizer for compensating for a fine frequency offset by detecting the pilot symbol from the demodulated data symbol stream.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

FIG. 1 is a diagram illustrating a structure of a general OFDM/CDMA system;

FIG. 2 is a diagram illustrating a data structure using pilot samples in a general OFDM/CDMA system;

FIG. 3 is a diagram illustrating a structure of a transmitter in an OFDM/CDMA system according to an embodiment of the present invention;

FIG. 4A is a diagram illustrating pilot symbol-inserted frame structure in an OFDM/CDMA system according to an embodiment of the present invention;

FIG. 4B is a diagram illustrating a guard interval-inserted frame structure in an OFDM/CDMA system according to an embodiment of the present invention;

FIG. 5 is a diagram illustrating a structure of a receiver in an OFDM/CDMA system according to an embodiment of the present invention;

FIG. 6 is a diagram illustrating a detailed structure of the first carrier synchronize of FIG. 5; and

FIG. 7 is a diagram illustrating a detailed structure of the second carrier synchronizer of FIG. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described herein below with reference to the accompanying drawings. In the following description, well-known functions or constructions are not described in detail since they would obscure the invention in unnecessary detail.

In an exemplary embodiment of the present invention, a guard interval and a pilot symbol are used to estimate a frequency offset in such actual states as timing error, common phase error and noises. A structure of a transmitter for inserting the guard interval and the pilot symbol before transmission will be described below with reference to FIG. 3.

A serial-to-parallel (S/P) converter 201 receives in series a data symbol, which is spread with a code of length N and comprised of N data samples, and outputs the N data samples in parallel. A pilot symbol inserter 203 receives in parallel the N data samples from the S/P converter 201, and inserts pilot symbols in a frame in a specific pattern before transmission. The pilot symbol inserter 203 can be comprised of means (not shown) for generating the pilot symbol and switching means (now shown) for switching the data symbol and the pilot symbol according to a specific pattern. The switching means can be comprised of a multiplexer. The pilot symbol inserter 203 can also be positioned in a preceding stage of the S/P converter 201. An inverse fast Fourier transform (IFFT) section 205 receives in parallel the N data samples output from the pilot symbol inserter 203, performs inverse fast Fourier transform on the received data samples, and outputs the IFFT-transformed OFDM symbol to a parallel-to-serial (P/S) converter 207. The IFFT-transformed OFDM symbol is comprised of N data samples. Since the N data samples of the OFDM symbol are OFDM-modulated in the data

symbol unit, those are different from the N data samples before the IFFT operation. The P/S converter 207 serializes the IFFT-transformed N data samples and outputs them to a guard interval inserter 209. The guard interval inserter 209 copies a part of the rear end of the OFDM symbol output from the P/S converter 207, and inserts it in the front of the data symbol. In the following description, it will be assumed that the number of data samples in the guard interval is N (the number of data samples) × 1/2.

A digital-to-analog converter (DAC) 213 converts the OFDM symbol output from the guard interval inserter 209 and then up-converts the converted OFDM symbol before transmission.

FIG. 4A illustrates a pilot symbol-inserted frame structure in an OFDM/CDMA system according to an embodiment of the present invention, wherein the hatched symbols #0 and #5 are the pilot symbols, and the pilot symbols are inserted at intervals of 4 data symbols. The pilot symbols can also be inserted in one frame at regular intervals or inserted at regular intervals without frame separation.

FIG. 4B illustrates a guard interval-inserted frame structure output from the guard interval inserter 209 of FIG. 3, in an OFDM/CDMA system according to an embodiment of the present invention.

In FIG. 4B, for the guard interval of each OFDM symbol, a part of the rear end of the corresponding OFDM symbol is copied and inserted in the front of the OFDM symbol. In the embodiment of the present invention, a length of the guard interval is determined as 1/2 the number N of the data samples.

FIG. 5 illustrates a structure of a receiver in an OFDM/CDMA system according to an embodiment of the present invention.

In actual circumstances, the receiver of the OFDM/CDMA system has the frequency offset, the common phase error, the noises and the timing error. The signals received in the actual circumstances should be modeled. As illustrated in FIG. 3, if it is assumed that the signal at the input end of the IFFT 205 in the transmitter of the OFDM/CDMA system is $X_m(k)$ and the signal passed the IFFT 205, in which the guard interval is not inserted yet, is $X_m[n]$, a signal FFT-transformed by the receiver after removing $y'_m[n]$ and the guard interval from an analog-to-digital converted signal will

be defined as $Y'_m[k]$ in the following description.

If a frequency offset per symbol is k_e [Hz/symbol], then a frequency offset per sample is k_e/N [Hz/sample] and a frequency offset $k_m[n]$ of an n^{th} sample of an m^{th} symbol is expressed by Equation (2) below.

$$k_m[n] = \frac{k_e}{N} m\{N+G\} + \frac{k_e}{N} n \quad \ldots\ldots. (2)$$

where G denotes the number of samples in the guard interval.

In the receiver, a signal $y_m[n]$ including the frequency offset, the common phase error and the noises is expressed by Equation (3) below, in which for convenience, the number of samples is given from –G to N-1.

$$\begin{aligned} y_m[n] &= X_m[n] \cdot e^{j2\pi k_m[n]} \cdot e^{jP_e} + W_m[n] \\ &= X_m[n] \cdot e^{\frac{j2\pi k_e[m\{N+G\}+n]}{N}} \cdot e^{jP_e} + W_m[n] \\ &= X_m[n] \cdot e^{j2\pi k_e \frac{n}{N}} \cdot e^{\frac{j2\pi k_e m\{N+G\}}{N}} \cdot e^{jP_e} + W_m[n] \quad \ldots\ldots. (3) \end{aligned}$$

where P_e denotes the common phase error and $W_m[n]$ denotes AWGN (Additive White Gaussian Noise) of the m^{th} symbol.

Now, the structure and operation of the receiver will be described with reference o FIG. 5. An analog-to-digital converter (ADC) 221 down-converts the analog signal transmitted from the transmitter and converts the down-converted analog signal to a digital OFDM symbol. In the following description, the signal output from the ADC 221 will be defined as $y'_m[n]$. A first carrier synchronizer 223 is a carrier synchronizer which uses the guard interval. The first carrier synchronizer 223 receives the OFDM symbol output from the ADC 221, detects a guard interval G of the FODM symbol and G data samples (hereinafter, referred to as copied data samples) at the rear end of the data symbol used to insert the guard interval, and performs frequency synchronization by compensating for the frequency offset of the OFDM symbol output from the ADC 221 using the guard interval and the data samples copied to generate the guard interval. In the embodiment of the present invention, the number G of the data

samples in the guard interval is 1/2 the number N of the data samples of the data symbol. If a signal of the guard interval, i.e., the guard interval comprised of the G data samples inserted in the front of the m^{th} OFDM symbol is defined as $G_m[n]$ and the last G data samples of the OFDM symbol, i.e., the data samples copied to create the guard interval is defined as $R_m[n]$, then $G_m[n]$ and $R_m[n]$ can be expressed by Equation (4) below.

$$G_m[n] = y_m[n-G] \cdot e^{\frac{j2\pi k_e[n-G]}{N}} \cdot e^{\frac{j2\pi k_e[n+G]}{N}} \cdot e^{jP_e} + W_m[n-G]$$
$$R_m[n] = y_m[n+N-G] \cdot e^{\frac{j2\pi k_e[n+N-G]}{N}} \cdot e^{\frac{j2\pi k_e[n+N+G]}{N}} \cdot e^{jP_e} + W_m[n+N-G] \quad \ldots (4)$$

A detailed description will be made of a carrier synchronizing operation using the guard interval of the first carrier synchronizer 223 in accordance with Equations (2) to (4). The first carrier synchronizer 223 detects phases of the $G_m[n]$ and $R_m[n]$, and calculates a phase difference between the detected phases of $G_m[n]$ and $R_m[n]$. The phase difference between $G_m[n]$ and Rm[n] is expressed by Equation (5) below.

$$\angle G_m[n] = \angle X_m[n-G] + \frac{2\pi k_e[n-G]}{N} + \frac{2\pi k_e m[N+G]}{N} + P_e + \angle W_m[n-G]$$
$$\angle R_m[n] = \angle X_m[n+N-G] + \frac{2\pi k_e[n+N-G]}{N} + \frac{2\pi k_e m[N+G]}{N} + P_e + \angle W_m[n+N-G]$$
$$\begin{aligned}\angle R_m[n] - \angle G_m[n] &= \angle X_m[n+N-G] - \angle X_m[n-G] \\ &\quad + \frac{2\pi k_e[n+N-G]}{N} - \frac{2\pi k_e[n-G]}{N} + \angle W_m[n+N-G] - W_m[n-G] \\ &= 2\pi k_e + \angle W_m[n+N-G] - \angle W_m[n-G] \quad \ldots\ldots. (5)\end{aligned}$$

In Equation (5), $X_m[n+N+G]$ and $X_m[n-G]$ are the identical signal, so that the phase difference is '0'.

When the phase difference between $G_m[n]$ and $R_m[n]$ is calculated from Equation (5), the first carrier synchronizer 223 calculates an average value of the phase difference using Equation (6) below. The first carrier synchronizer 223 performs carrier synchronization by approximately compensating for the frequency offset of the data input from the ADC 221 based on the calculated average value.

$$k_e = \frac{avg\{\angle R_m[n] - \angle G_m[n]\}}{2\pi} \quad \ldots\ldots.(6)$$

Here, if there exists a timing error, there is a case where Equations (2) to (6) are not correct. If the timing error such as an FFT start point detection error and a timing frequency offset is n_e, a signal $y'_m[n]$ including the timing error can be expressed by Equation (7) below.

$$\begin{aligned} y'_m &= y_m[n-n_e] \\ &= X_m[n-n_e] \cdot e^{\frac{jwpik_e[n-n_e]}{N}} \cdot e^{\frac{j2\pi k_e m[n+G]}{N}} \cdot e^{jP_e} + W_m[n-n_e] \quad \ldots.(7) \end{aligned}$$

Here, $y'_m[n]$ includes data samples of the $(m-1)^{th}$ OFDM symbol or the $(m+1)^{th}$ OFDM symbol according to the value of n_e. On the above assumption, the phase difference of the respective samples is calculated by Equation (8) below.

$$\begin{aligned} \angle R_m[n] - \angle G_m[n] &= \angle X_m[n+N-G-n_e] - \angle X_m[n-G-n_e] \\ &+ \frac{2\pi k_e[n+N-G-n_e]}{N} - \frac{2\pi k_e[n-G-n_e]}{N} + \angle W_m[n+N-G-n_e] - W_m[n-G-n_e] \\ &= 2\pi k_e + \angle W_m[n+N-G-n_e] - \angle W_m[n-G-n_e] \quad \ldots\ldots.(8) \end{aligned}$$

In Equation (8), $G_m[n]$ and $R_m[n]$ have the values shifted by n_e from their original values, so that the range of $X_m[n+N+G-n_e]$ and $X_m[n-G-n_e]$ becomes $n=n_e$, n_e+1, .., G-1, and n=0, 1, 2, .., $G-n_e-1$ for the negative number. Hence, if an approximate range of the timing error of the system is known, the frequency offset is calculated in the interval from which the range is excluded. For example, if the maximum timing error does not exceed 'a', the frequency offset can be estimated using Equation (9) below by calculating the phase difference in the interval of n=a, a+1, .., G-a-2, G-a-1, and calculating the average value.

$$k_e = \frac{avg[\angle R_m[n] - \angle G_m[n]]}{2\pi} \quad \ldots\ldots.(9)$$

Equations (2) to (9) are used when the first carrier synchronizer 223 performs carrier synchronization by estimating the approximate frequency offset. The first carrier synchronizer 223 has the better performance when the used guard interval becomes

longer and the timing error of the system has the narrower range. Otherwise, the frequency offset measuring interval becomes shorter, so that the first carrier synchronizer is more affected by the noises and has a difficulty in correctly measuring the frequency offset. After the approximate carrier synchronization, a guard interval remover 225 removes the guard interval from the received data output from the first carrier synchronizer 223 and outputs the guard interval-removed data to a fast Fourier transform (FFT) section 227. The FFT 227 receives the guard interval-removed OFDM symbol, performs the FFT operation on the received OFDM symbol and outputs the original data symbol.

A second carrier synchronizer 229 receives the data symbol FFT-transformed by the FFT 227 and performs fine carrier synchronization on the received data symbol. Specifically, the second carrier synchronizer 229 detects the pilot symbol of the symbol unit from the data symbol stream, and calculates a phase of the detected pilot symbol. The second carrier synchronizer 229 estimates the fine frequency offset by calculating a phase difference between the calculated phase of the pilot symbol and a known phase of a pilot symbol. After estimation of the fine frequency offset, the second carrier synchronizer 229 performs fine carrier synchronization by compensating for the estimated fine frequency offset.

An operation of the second carrier synchronizer 229 will be mathematically described below. For the data symbol output from the FFT 227, a frequency offset according to the FFT characteristics is a shift timing error of the signal and is converted to a variation of the phase. This can be expressed by Equation (10) below.

$$\begin{aligned} y'_m[k] &= X_m[k-k_i]\cdot e^{\frac{j2\pi[k-k_i]n_e}{N}}\cdot e^{\frac{j2\pi k_i m[N+G]}{N}}\cdot e^{jP_e}+W_m[k-k_i] \\ &= X_m[k-k_i]\cdot e^{\frac{j2\pi k n_e}{N}}\cdot e^{-\frac{j2\pi k_i n_e}{N}}\cdot e^{-\frac{j2\pi k_i m[N+G]}{N}}\cdot W_m[k-k_i] \qquad \ldots\ldots(10) \end{aligned}$$

where k_i denotes the fine frequency offset.

If only the pilot symbol is detected from the received data, the range of m is 0, l-1, 2l-1, 3l-1, ..., where l denotes a period for inserting the pilot symbol of the symbol unit.

The phase difference of the received pilot symbol is calculated by Equation (11) below.

$$\angle y'_m[k] = \angle X_m[k-k_i] + \frac{2\pi n_e}{N}k - \frac{2\pi n_e k_i}{N} + \frac{2\pi k_i m[N+G]}{N} + P_e + \angle W_m[k-k_i] \quad \ldots.(11)$$

In Equation (11), the second term is expressed in terms of a specific variation of the phase according to an index k, the next three terms are expressed in terms of a constant phase offset, and the last term is expressed in terms of a variation of the phase. If the transmitter continuously uses the same pilot symbol and the time error, the common phase error and the frequency offset are identical during the pilot symbol insertion period, then a phase difference between consecutive two pilot symbols $Y_{mpi}'(k)$ and Y_{mpi+1} is calculated by

$$\begin{aligned} diff_{phase} &= \angle y'_{m\pi+1}[k] - \angle y'_{m\pi}[k] \\ &= \angle X_{m\pi+1}[k-k_i] - \angle X_{m\pi}[k-k_i] + \frac{2\pi k_i m_{\pi+1}[N+G]}{N} - \frac{2\pi k_i m_\pi[N+G]}{N} \\ &\quad + \angle W_{m_{n+1}}[k-k_i] - \angle W_{m_n}[k-k_i] \quad \ldots\ldots.(12) \end{aligned}$$

If the transmitter uses the same pilot symbol as stated above, the first term and the second term have the same value. Hence, Equation (12) can be expressed by Equation (13) below.

$$\begin{aligned} diff_{phase} &= [m_{\pi+1} - m_\pi]\frac{2\pi k_i[N+G]}{N} + \angle W_{m_{\pi+1}}[k-k_i] - \angle W_{m_\pi}[k-k_i] \\ &= I\frac{2\pi k_i[N+G]}{N} + \angle W_{m_{\pi+1}}[k-k_i] - \angle W_{m_\pi}[k-k_i] \quad \ldots\ldots.(13) \end{aligned}$$

In Equation (13), the first term is expressed in terms of a constant for N samples of one pilot symbol, and the other terms are expressed in terms of a variation due to the noises. Hence, by calculating an average value of the phase differences for N samples, it is possible to obtain the constant of the first term, from which the influence of the noises is almost removed. From this value, it is possible to calculate a fine frequency offset k_i in accordance with Equation (14) below.

$$k_e = \frac{avg\ diff_{phase} \times N}{2\pi[N+G] \times I} \quad \ldots\ldots\ (14)$$

After calculating the fine frequency offset using Equation (14), the second carrier synchronizer 229 performs carrier synchronization by compensating for a frequency offset of the OFDM symbol based on the calculated frequency offset, and provides its output to a despreader 231. The despreader 231 despreads the fine frequency-synchronized received data.

The detailed structure of the first carrier synchronizer 223 and the second carrier synchronizer 229 will be described with reference to FIGS. 6 and 7. Specifically, FIG. 6 illustrates the detailed structure of the first carrier synchronizer of FIG. 5, and FIG. 7 illustrates the detailed structure of the second carrier synchronizer of FIG. 5.

In FIG. 6, a guard interval detector 301 receives the OFDM symbol stream including the respective guard intervals, output from the ADC 221 of FIG. 5, detects the respective guard intervals $G_m[n]$ included in the OFDM symbol stream, and calculates phases of the respective guard intervals $G_m[n]$. A copied sample detector 303 receives the OFDM symbol stream, detects data samples (hereinafter, referred to as "copied data samples") of the OFDM symbol copied to create the guard intervals $G_m[n]$ to be detected, and calculates phases of the copied data samples. In Equations (2) to (9), the copied data samples are indicated by $R_m[n]$. A phase difference detector 305 calculates phase differences between the data samples of the guard intervals $G_m[n]$ output from the guard interval detector 301 and the copied data samples $R_m[n]$ output from the copied sample detector 303, and outputs the detected phase differences to an averager 307. The averager 307 calculates an approximate frequency offset by averaging the phase differences output from the phase difference detector 305 in a unit of G (=R), and outputs an approximate frequency offset compensation signal to a first frequency offset compensator 309. The first frequency offset compensator 309 receives the OFDM symbol stream including the guard intervals output from the ADC 221, and compensates for the approximate frequency offset of the OFDM symbol stream according to the approximate frequency offset compensation signal output from the averager 307.

In FIG. 7, a pilot symbol detector 311 receives IFFT-transformed received data output from the FFT 227, and detects a pilot symbol included in the received data. The

pilot symbol output from the pilot symbol detector 311 is applied to a delay 312 and a phase difference detector 313. The delay 312 buffers the detected pilot symbol, delays the buffered pilot symbol by the pilot symbol insertion period, and then outputs the delayed pilot symbol to a phase difference detector 313. The phase difference detector 313 receives the pilot symbol detected by the pilot symbol detector 311 and the pilot symbol delayed by the symbol insertion period from the detected pilot symbol, output from the delay 312, calculates phase differences between the corresponding samples of the two pilot symbols, and outputs the calculated phase differences to an averager 314. The averager 314 estimates the fine frequency offset by calculating an average value of the phase differences in the pilot symbol period. After estimation of the fine frequency offset, the averager 314 outputs a fine frequency offset compensation signal for the fine frequency offset to a second offset compensator 315. The second offset compensator 315 receives the FFT-transformed received data from the FFT 327, and compensates for a fine frequency offset of the received data according to the fine frequency offset compensation signal output from the averager 314.

As described above, the invention can compensate for a frequency offset even in a situation where the timing error is not compensated for, and increase the accuracy of frequency offset estimation by removing the influence of the variation due to the noises.

WHAT IS CLAIMED IS:

1. An apparatus of compensating for a frequency offset using a pilot symbol for a transmitter in an OFDM/CDMA (Orthogonal Frequency Division Multiplexing/Code Division Multiple Access) system including a receiver for performing fine frequency synchronization using a pilot symbol, comprising:

a pilot symbol inserter for receiving a spread data symbol stream and inserting a pilot symbol in a symbol unit according to a predetermined pattern.

2. An apparatus of compensating for a frequency offset using a pilot symbol for a transmitter in an OFDM/CDMA system including a receiver for performing fine frequency synchronization using a pilot symbol, comprising:

a pilot symbol inserter for receiving a spread data symbol steam, and inserting a pilot symbol at intervals of predetermined data symbols;

a serial-to-parallel (S/P) converter for receiving the pilot symbol-inserted data symbol stream, and outputting N data samples of a symbol unit in parallel;

an inverse fast Fourier transform (IFFT) section for performing an IFFT operation on the N data samples;

a parallel-to-serial (P/S) converter for serializing the IFFT-transformed N data samples and outputting an OFDM symbol; and

a guard interval inserter for copying a part of the N data samples of the OFDM symbol and inserting the copied data samples in the front of the OFDM symbol.

3. An apparatus of compensating a frequency offset using a pilot symbol for a receiver in an OFDM/CDMA system including a transmitter for inserting a pilot symbol in a data symbol of frame unit in a specific pattern before transmission, comprising:

a carrier synchronizer for compensating for a fine frequency offset using the pilot symbol inserted in the specific pattern out of the IFFT-transformed data symbol stream.

4. The apparatus as claimed in claim 3, wherein the carrier synchronizer comprises:

a pilot symbol detector for detecting a pilot symbol from an OFDM-demodulated data symbol stream;

a delay for delaying the detected pilot symbol by a predetermined time;

a phase difference detector for detecting a phase of the pilot symbol output from the pilot symbol detector and a phase of the delayed pilot symbol output from the delay, and calculating a phase difference between the two pilot symbols;

an averager for calculating a fine frequency offset by averaging the phase differences in a frame unit and outputting a second frequency offset compensation signal according to the fine frequency offset; and

a second frequency offset compensator for compensating for a fine frequency offset of the demodulated data symbol according to the second frequency offset compensation signal.

5. An apparatus of compensating for a frequency offset using a pilot symbol for a receiver in an OFDM/CDMA system including a transmitter for inserting a pilot symbol in a data symbol stream of a frame unit in a specific pattern before transmission, comprising:

a first carrier synchronizer for receiving an OFDM symbol stream including received guard intervals and performing approximate frequency synchronization on the received OFDM symbol stream using the guard interval;

a guard interval remover for removing the guard intervals from the OFMD symbol streams after performing frequency synchronization;

a fast Fourier transform (FFT) section for performing an FFT operation on the guard interval-removed OFDM symbol and outputting the data symbol; and

a second carrier synchronizer for compensating for a fine frequency offset using the pilot symbol inserted in the data symbol stream in the specific pattern.

6. The apparatus as claimed in claim 5, wherein the first carrier synchronizer comprises:

a guard interval detector for detecting a guard interval from the OFDM symbol stream;

a copied sample detector for detecting data samples copied to create the detected guard interval, from the OFDM symbol stream;

a phase difference detector for calculating a phase of the data samples of the detected guard interval and a phase of the copied data samples, and calculating a phase difference between the two data samples;

an averager for calculating a frequency error by averaging the phase differences output from the phase difference detector in the frame unit, and outputting a first frequency offset compensation signal according to the frequency offset; and

a first frequency offset compensator for compensating for a frequency offset of the OFDM symbol according to the first frequency offset compensation signal.

7. The apparatus as claimed in claim 5, wherein the second carrier synchronizer comprises:

a pilot symbol detector for detecting the pilot symbol from the data symbol stream;

a delay for delaying the pilot symbol by a pilot symbol insertion period;

a phase difference detector for detecting a phase of a pilot symbol output from the pilot symbol detector and a phase of the delayed pilot symbol output from the delay, and calculating a phase difference between the two pilot symbols;

an average for calculating a fine frequency offset by averaging the phase differences received in the frame unit, and outputting a second frequency offset compensation signal according to the fine frequency offset; and

a second frequency offset compensator for compensating a fine frequency error of the demodulated data symbol according to the second frequency offset compensation signal.

8. The apparatus as claimed in claim 7, wherein the fine frequency offset is calculated by

$$k_e = \frac{avg\ diff_{phase} \times N}{2\pi[N+G] \times I}.$$

FIG. 1

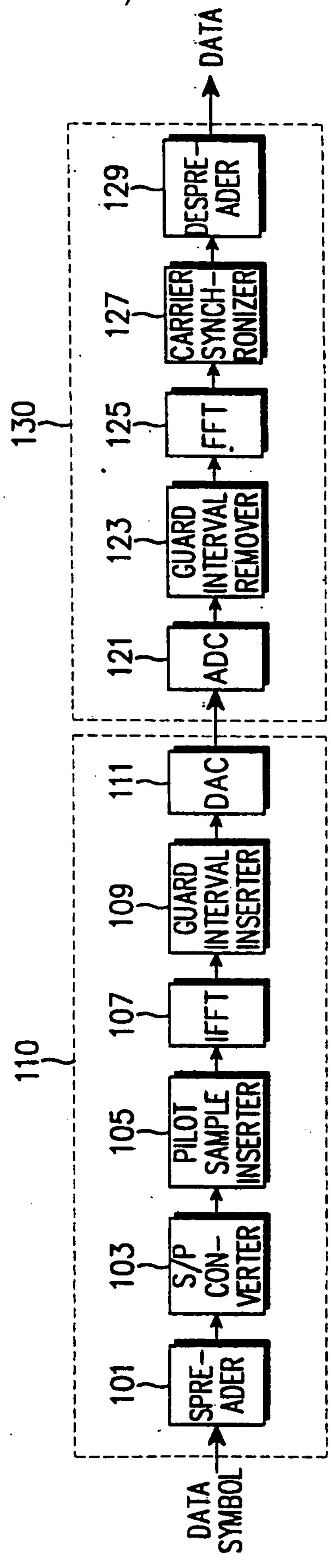

DATA SYMBOL
101
SPREADER
103
S/P CONVERTER
105
PILOT SAMPLE INSERTER
107
IFFT
109
GUARD INTERVAL INSERTER
111
DAC
110
121
ADC
123
GUARD INTERVAL REMOVER
125
FFT
127
CARRIER SYNCHRONIZER
129
DESPREADER
130
DATA

FIG. 2

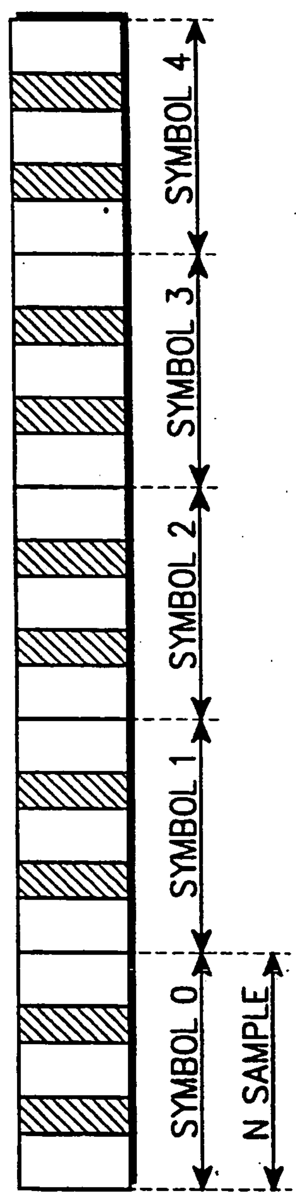
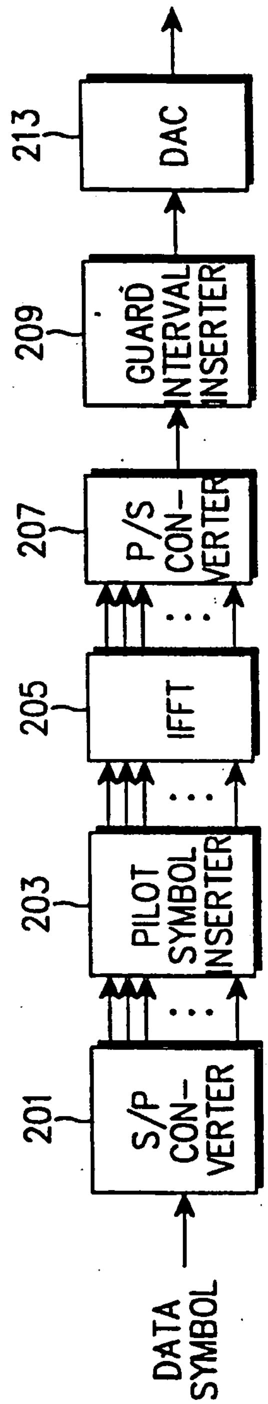


FIG. 3


DATA SYMBOL
201
S/P CON-VERTER
203
PILOT SYMBOL INSERTER
205
IFFT
207
P/S CON-VERTER
209
GUARD INTERVAL INSERTER
213
DAC

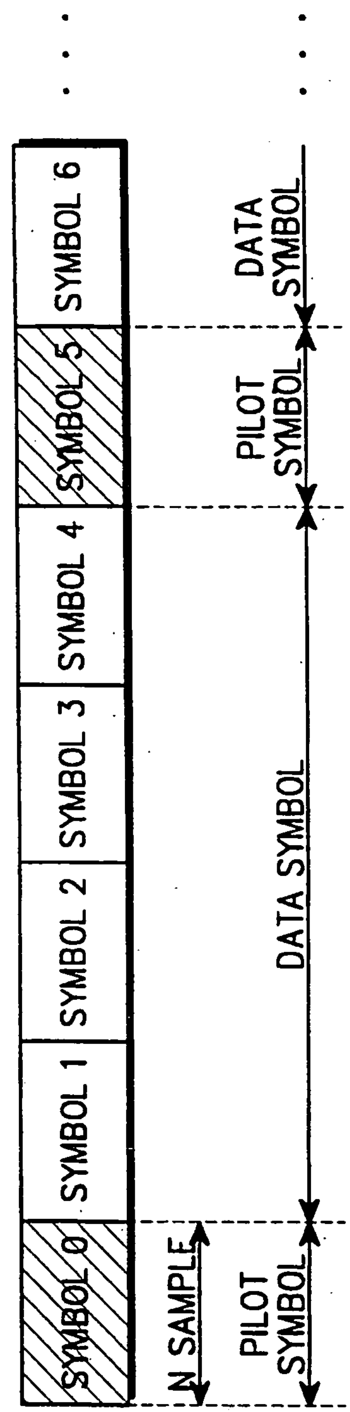

SYMBOL 0
SYMBOL 1
SYMBOL 2
SYMBOL 3
SYMBOL 4
SYMBOL 5
SYMBOL 6
N SAMPLE
PILOT SYMBOL
DATA SYMBOL
PILOT SYMBOL
DATA SYMBOL

FIG. 4A

FIG. 4B

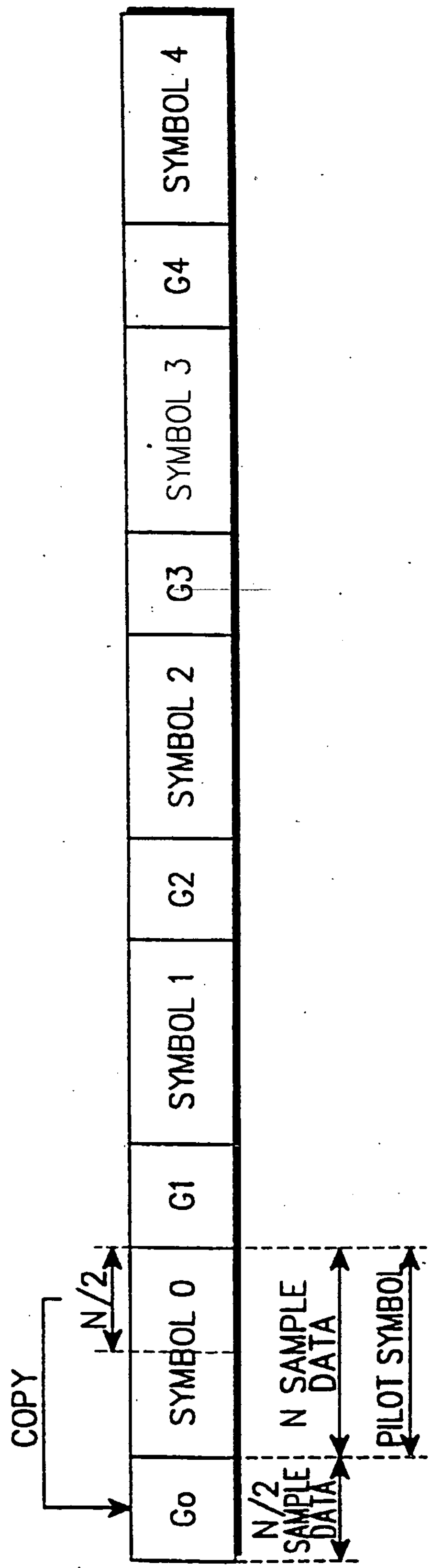

SYMBOL 4
G4
SYMBOL 3
G3
SYMBOL 2
G2
SYMBOL 1
G1
SYMBOL 0
Go
COPY
N/2
N SAMPLE DATA
PILOT SYMBOL
N/2 SAMPLE DATA

FIG. 5

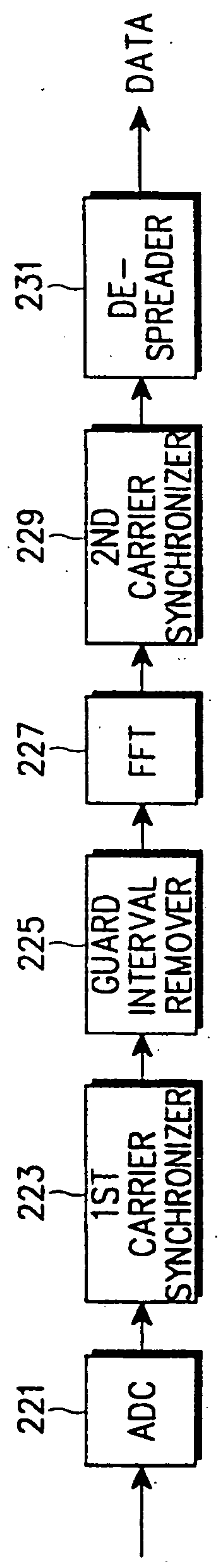

221
ADC
223
1ST CARRIER SYNCHRONIZER
225
GUARD INTERVAL REMOVER
227
FFT
229
2ND CARRIER SYNCHRONIZER
231
DE-SPREADER
DATA

FIG. 6

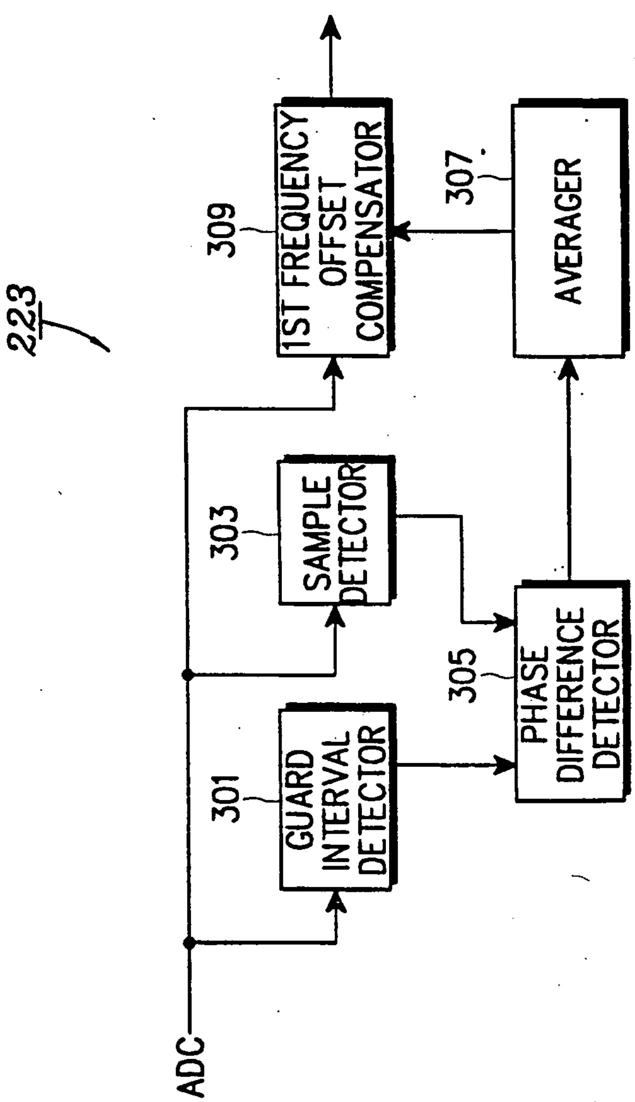
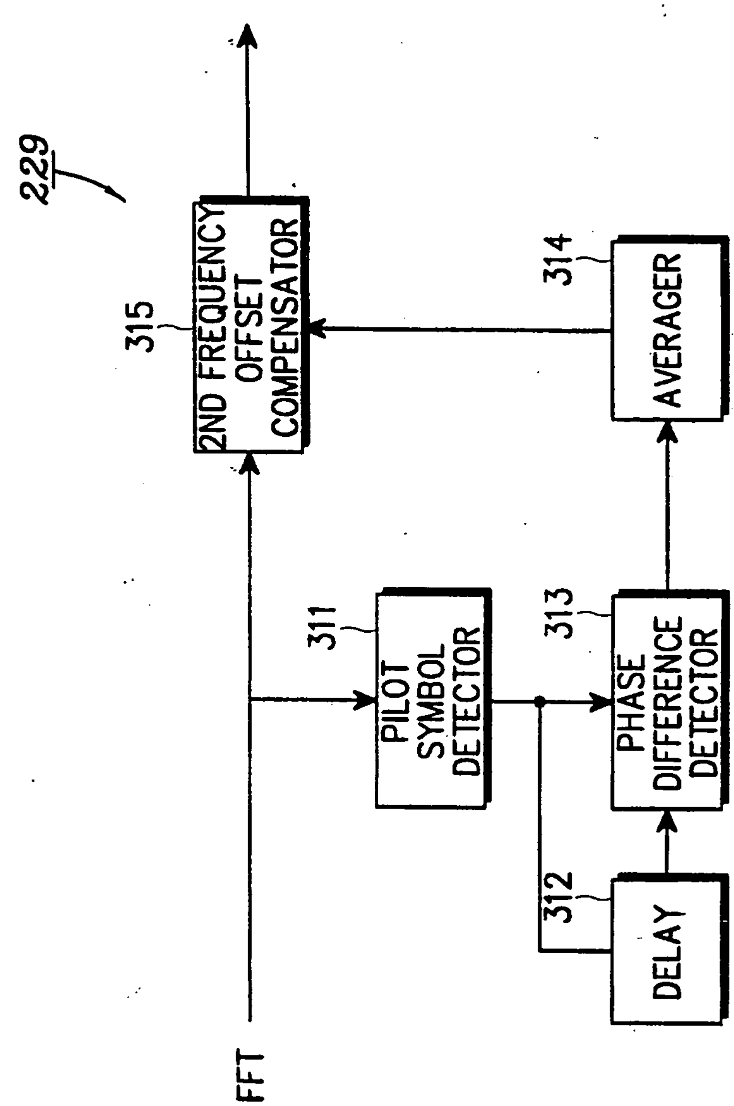

223
ADC
301
GUARD INTERVAL DETECTOR
303
SAMPLE DETECTOR
305
PHASE DIFFERENCE DETECTOR
307
AVERAGER
309
1ST FREQUENCY OFFSET COMPENSATOR

FIG. 7


229
2ND FREQUENCY OFFSET COMPENSATOR
315
AVERAGER
314
PILOT SYMBOL DETECTOR
311
PHASE DIFFERENCE DETECTOR
313
DELAY
312
FFT

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H04J 11/00,

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimun documentation searched (classification system followed by classification symbols)

KE, JP, US, EP classes as above

Documentation searched other than minimun documentation to the extent that such documents are included in the fileds searched

Korean Patents and applications for inventions since 1975
Korean Utility models and applications for Utility models since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search trerms used)

NPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KE 10-99-003705(DAWOO ELECTRIC) 15 JAN. 1999 abstract, col.3 line 26 ~ col. 9 fig 3, 5, 6, 9, 10	1 ~ 8
A	JP 8-79217(VICTOR CO.) 22 MAR. 1996 abstract, fig	1 ~ 8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevence; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevence; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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Government Complex-Taejon, Dunsan-dong, So-ku, Taejon
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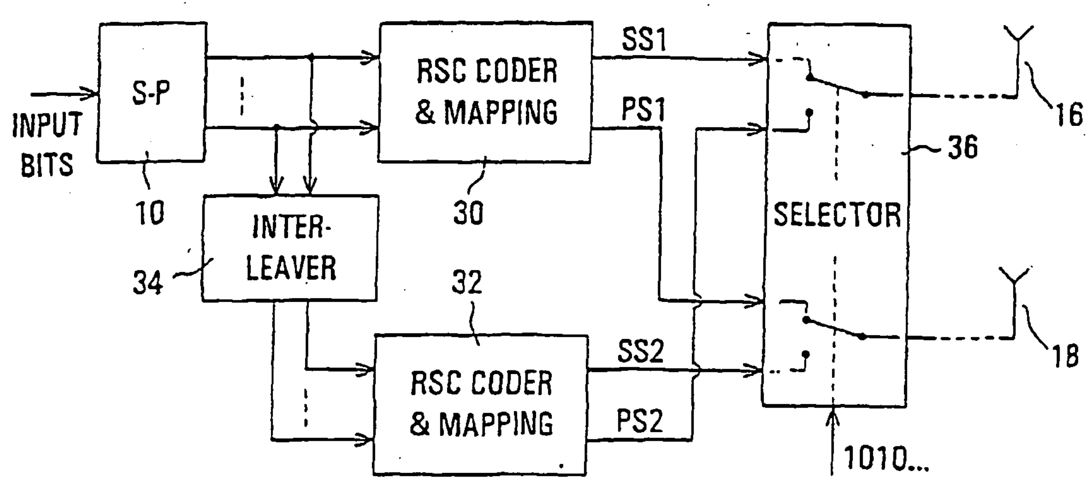
[Continued on next page]

(54) Title: METHODS AND APPARATUS FOR TURBO SPACE-TIME TRELLIS CODING



(57) Abstract: Space-time diversity using a plurality of transmit antennas (16, 18) is provided with a turbo coding arrangement comprising two recursive systematic convolutional coders (30, 32), to one of which input bits are supplied directly and to the other of which the information bits are supplied after interleaving (34) of bit groups for respective symbol intervals. Symbols produced by the coders and comprising systematic and parity information are supplied to paths to the antennas alternately in successive symbol intervals to provide the space-time diversity. Arrangements are described for 2 and 4 antennas and for various convolutional codes, and an iterative decoder is also described.

WO 02/43314 A1

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

METHODS AND APPARATUS FOR TURBO SPACE-TIME TRELLIS CODING

This invention relates to communications, for example for a cellular wireless communications system, using a combination of so-called turbo, space-time (ST), and trellis coding (TC) or trellis coded modulation (TCM) techniques.

Background of the Invention

As is well known, wireless communications channels are subject to time-varying multipath fading, and it is relatively difficult to increase the quality, or decrease the effective error rate, of a multipath fading channel. While various techniques are known for mitigating the effects of multipath fading, several of these (e.g. increasing transmitter power or bandwidth) tend to be inconsistent with other requirements of a wireless communications system. One technique which has been found to be advantageous is antenna diversity, using two or more antennas (or signal polarizations) at a transmitter and/or at a receiver of the system.

In a cellular wireless communications system, each base station typically serves many remote (fixed or mobile) units and its characteristics (e.g. size and location) are more conducive to antenna diversity, so that it is desirable to implement antenna diversity at least at a base station, with or without antenna diversity at remote units. At least for communications from the base station in this case, this results in transmit diversity, i.e. a signal is transmitted from two or more transmit antennas.

S. M. Alamouti, "A Simple Transmit Diversity Technique for Wireless Communications", IEEE Journal on Selected Areas in Communications, Vol. 16, No. 8, pages 1451-1458, October 1998 describes a simple transmit diversity scheme using space-time block coding (STBC). For the case of two transmit antennas, complex symbols s0 and -s1* are successively

transmitted from one antenna and simultaneously complex symbols s1 and s0* are successively transmitted from the other antenna, where * represents the complex conjugate. These transmitted symbols constitute what is referred to as a space-time block.

It is also known to use various coding schemes in order to enhance communications. Among such schemes, it has been recognised that so-called turbo coding (parallel concatenated convolutional coding) enables iterative decoding methods to achieve results which are close to the Shannon limit for AWGN (additive white Gaussian noise) communication channels. A turbo coder uses two, typically identical, recursive systematic convolutional (RSC) component coders, signals to be transmitted being supplied directly to one of the component coders and via an interleaver to the other of the component coders. Accordingly, it would be desirable to combine turbo and space-time coding techniques in the same transmitter.

V. Tarokh et al., "Space-Time Codes for High Data Rate Wireless Communication: Performance Criterion and Code Construction", IEEE Transactions on Information Theory, Vol. 44, No. 2, pages 744-765, March 1998 describes various convolutional, or trellis, codes which can be used with two or more transmit antennas to provide the advantages of trellis (convolutional) coding and space-time coding. Although these codes are considered optimal for maximum diversity gain, they are not necessarily optimal for coding gain. Furthermore, these codes are non-recursive. In contrast, it is well established that the best efficiency for turbo coding is achieved using recursive codes. Consequently, the codes described by Tarokh et al. are not suitable for use in a turbo coding arrangement.

P. Robertson et al., "Bandwidth-Efficient Turbo Trellis-Coded Modulation Using Punctured Component Codes", IEEE Journal on Selected Areas in Communications, Vol. 16, No. 2, pages 206-218, February 1998 describes a turbo coder using Ungerboeck and multidimensional TCM component codes, in which the interleaver operates on groups each of m information bits. For each step corresponding to a group of m information bits, a signal mapper associated with each component coder produces n symbols, where n=D/2 and D is the signal set dimensionality; for example D=2 or 4 and n=1 or 2. An n-symbol de-interleaver de-interleaves output symbols from the second component coder, and a selector alternately for successive steps selects symbols output from the first component coder and symbols from the de-interleaver and supplies them to a single output path. This arrangement does not provide transmit diversity and this document is not concerned with space-time coding.

G. Bauch, "Concatenation of Space-Time Block Codes and "Turbo"-TCM", Proceedings of the International Conference on Communications, ICC'99, pages 1202-1206, June 1999 describes two types of turbo trellis coded modulation (TCM) coder, whose output is supplied to a space-time block coder, so that the turbo-TCM and STBC arrangements are simply concatenated with one another. One of these two types of turbo TCM coder is as described by Robertson et al. (to which reference is made for details) as discussed above using Ungerboeck codes and providing one symbol at the output of the mapping function, but the Bauch illustration of this does not show the symbol de-interleaver. This Bauch publication does not discuss multidimensional component codes.

A continuing need exists to provide further improvements in wireless communications.

Summary of the Invention

According to one aspect, this invention provides a method of providing space-time diversity for information to be transmitted from a plurality T of antennas, comprising the steps of: in each of a plurality of successive symbol intervals, producing T symbols comprising systematic information and parity information at outputs of each of two recursive systematic convolutional coders, to one of which coders input bits are supplied directly and to the other of which coders said information bits are supplied after interleaving of bit groups for respective symbol intervals in an interleaving block; and selecting first and second different mappings, each of T symbols from said symbols produced at the outputs of the coders, in respective alternating symbol intervals for supply to the T antennas to provide said space-time diversity, the interleaving and mappings being arranged so that systematic information is selected for all of the input bits in the interleaving block.

Preferably the first mapping selects the T symbols from one of the coders and the second mapping selects the T symbols from the other of the coders.

In an embodiment of the invention described below, T=2 and in each symbol interval each coder produces a systematic information symbol and a parity information symbol, the first mapping provides the systematic information symbol and the parity information symbol from one of the coders for supply respectively to first and second antennas, and the second mapping provides the systematic information symbol and the parity information symbol from the other of the coders for supply respectively to the second and the first antennas. Thus this is an example of a case in which T is even and in each symbol interval each coder produces T/2 systematic information symbols and T/2 parity information symbols.

Alternatively, the T symbols produced by each coder in each symbol interval can include at least one symbol comprising systematic and parity information.

The method may also include the step of changing a phase of symbols from the two coders relative to one another, in particular providing a phase rotation of $\pi/2$ for symbols at the output of one of the coders. This can be particularly desirable when t>2, for example when T=4.

Preferably the interleaved bit groups each comprise m bits where m is an integer, and symbols produced at the outputs of the coders comprise M-PSK symbols where $M=2^m$.

Another aspect of the invention provides a coding arrangement comprising: first and second recursive systematic convolutional coders each arranged to produce a plurality of T symbols in each of a plurality of successive symbol intervals from m bits supplied thereto, where m is an integer; an interleaver arranged to interleave groups each of m input bits within an interleaving block with a mapping of even-to-even and odd-to-odd, or even-to-odd and odd-to-even, positions; input bits supplied to the first coder and to the interleaver, and interleaved bits supplied from the interleaver to the second coder; and a selector arranged to supply different ones of the T symbols from the coders in alternate symbol intervals to respective ones of T output paths, the T symbols selected in each of the alternating symbol intervals including all of the systematic information from a respective one of the coders.

Thus the method and coding arrangement of the invention provide a desirable combination of turbo coding with recursive systematic convolutional component coders and space-time coding for transmit diversity.

The invention also provides a decoding arrangement for iteratively decoding received symbols coded by the coding arrangement recited above, comprising: first and second soft output decoders for decoding the coding by said first and second recursive systematic convolutional coders respectively, in response to an input vector and soft input information; an interleaver corresponding to the interleaver of the coder, arranged to couple soft output information from the first decoder as soft input information to the second decoder; a de-interleaver converse to said interleavers, arranged to couple soft output information from the second decoder as soft input information to the first decoder; and a selector arranged to supply a received signal vector and a zero input vector alternately in successive symbol intervals as the input vector to the first and second decoders.

The invention further provides a method of iteratively decoding a received signal comprising symbols coded by the method recited above, comprising the steps of: supplying a received signal vector and a zero input vector alternately in successive symbol intervals as input vectors to two decoders for decoding the coding by said two recursive systematic convolutional coders respectively; interleaving, in the same manner as in the method of coding, a soft output of one of the decoders, corresponding to said one of the coders, to provide a soft input to the other of the decoders; and de-interleaving, conversely to the interleaving, a soft output of said other of the decoders to provide a soft input to said one of the decoders.

Brief Description of the Drawings

The invention will be further understood from the following description with reference to the accompanying drawings, in which by way of example:

Fig. 1 illustrates parts of a known space-time block code (STBC) transmitter;

Fig. 2 illustrates a known signal point constellation for QPSK symbols;

Fig. 3 illustrates a known turbo coder;

Fig. 4 illustrates parts of a turbo space-time trellis coded modulation (STTCM) coding arrangement for a transmitter using two transmit antennas, in accordance with an embodiment of this invention;

Fig. 5 illustrates a general form of convolutional or trellis coder;

Fig. 6 illustrates a 4-state trellis coder which can be used in the arrangement of Fig. 4;

Fig. 7 illustrates an 8-state trellis coder which can be used in the arrangement of Fig. 4;

Fig. 8 illustrates a 16-state trellis coder which can be used in the arrangement of Fig. 4;

Fig. 9 illustrates a 4-state trellis coder for use in a turbo STTCM coding arrangement for a transmitter having four transmit antennas;

Fig. 10 illustrates parts of a coding arrangement for a transmitter in which the coder of Fig. 9 can be used in accordance with another embodiment of this invention; and

Fig. 11 illustrates parts of a receiver and decoding arrangement for use with the arrangement of Fig. 4 or Fig. 10.

Detailed Description

Referring to the drawings, Fig. 1 illustrates parts of a known space-time block code (STBC) transmitter. For simplicity and clarity in this and other figures of the drawings, only those parts are shown which are necessary for a full understanding of the prior art and embodiments of this invention.

The transmitter of Fig. 1 includes a serial-to-parallel (S-P) converter 10, an M-PSK mapping function 12, and a space-time block coder (STBC) 14 providing outputs, via transmitter functions such as up-converters and power amplifiers not shown but represented in Fig. 1 by dashed lines, to at least two antennas 16 and 18 which provide transmit diversity. The S-P converter 10 is supplied with input bits of information to be communicated and produces output bits on two or more parallel lines to the M-PSK mapping function 12, which produces from the parallel bits sequential symbols x_1, x_2, ... of an equal-energy signal constellation.

For example, as shown in Fig. 1 the mapping function 12 may provide a Gray code mapping of in each case 2 input bits from the S-P converter 10 to respective ones of M=4 signal points of a QPSK (quadrature phase shift keying) signal point constellation as illustrated in Fig. 2, the signal points being identified as symbols 0 to 3 respectively. For simplicity and convenience, Gray code QPSK mapping is assumed throughout the following description, but it can be appreciated that the mapping function 12 can provide any desired mapping to a signal point constellation with any desired number M of phase states; for example M=2 (for which the S-P converter 10 is not required), 4, or 8.

The QPSK symbols x_1, x_2, ..., represented by complex numbers, are supplied to the STBC 14, which for simplicity is

shown in Fig. 1 as having two outputs for the respective transmit antennas 16 and 18, but may instead have more than two outputs for a corresponding larger number of transmit antennas. For the case of two antennas as shown, the STBC 14 forms a space-time block of symbols, as represented in Fig. 1, from each successive pair of symbols x_1 and x_2 supplied to its input.

More particularly, the STBC function is represented by a T-by-T orthogonal matrix H_x, where T is the number of transmit antennas and hence symbol outputs of the STBC 14. For the case of T=2 as represented in Fig. 1,

$$H_x(x_1,x_2)=\begin{bmatrix} x_1 & x_2 \\ -x_2* & x_1* \end{bmatrix}$$

In accordance with this matrix H_x, for each pair of PSK symbols x_1 and x_2 supplied to the input of the STBC 14, in a first symbol interval the antenna 16 is supplied with the symbol x_1 and the second antenna 18 is supplied with the symbol x_2, and in a second symbol interval the first antenna 16 is supplied with the symbol $-x_2*$ and the second antenna 18 is supplied with the symbol x_1*, where * denotes the complex conjugate. Thus both PSK symbols in each pair are transmitted twice in different forms, from different antennas and at different times to provide both space and time diversity. It can be seen that each column of the matrix H_x indicates the symbols transmitted in successive intervals from a respective antenna, and each row represents a respective symbol transmission interval.

Referring to Fig. 3, a known turbo (parallel concatenated convolutional) coder comprises two recursive systematic convolutional (RSC) coders 20 and 22 which are referred to as the constituent or component codes of the turbo coder, an interleaver 24, and a selector 26. Input bits are supplied to the input of one coder 20, which produces at its outputs both systematic bits S1, which are the same as the input bits, and parity bits P1. The input bits are also

supplied to and interleaved by the interleaver 24, and the interleaved bits are supplied to the input of the other coder 22, which produces at its outputs both systematic bits S2, which are the same as the interleaved input bits, and parity bits P2. The outputs of the two coders 20 and 22 are supplied to inputs of the selector 26, except that typically and as shown in Fig. 3 the systematic bit output of the coder 22 is not connected because the interleaved bits at this output are never selected by the selector 26.

The selector 26 selects all of the systematic bits S1, and some or all of the parity bits P1 and P2 from the coders 20 and 22 respectively, and supplies them to an output of the turbo coder as output bits. The selection of parity bits depends upon the rate of the coder. For example, for a rate 1/3 (3 output bits for each input bit) coder, the selector 26 can select all of the parity bits P1 and P2. For a rate 1/2 (2 output bits for each input bit) coder, the selector 26 can alternately select the parity bits P1 and P2, so that only half of the parity bits P1 and half of the parity bits P2 are output, this process being referred to as puncturing.

In the turbo-TCM arrangement (Robertson et al.) referred to in the Background of the Invention, the interleaver 24 operates on groups each of m bits which are mapped at the output of each component coder (20, 22) into, for example, a PSK symbol combining the systematic and parity information. The symbols from the second component coder (22) are de-interleaved by a symbol de-interleaver, and the output selector alternately selects the symbols output from the first component coder (20) and the de-interleaver. The interleaver (and consequently also the de-interleaver) in this case must provide an even-to-even and odd-to-odd (or even-to-odd and odd-to-even) position mapping.

In the concatenated SBTC and turbo code (Bauch) arrangements referred to in the Background of the Invention, in essence the output bits of a turbo coder such as that of Fig. 3 are supplied as input bits to a space-time block coder such as that of Fig. 1, or the output symbols from a turbo-TCM coder as described by Robertson et al. are supplied as input symbols to an STBC coder 14 as described above with reference to Fig. 1.

Fig. 4 illustrates parts of a turbo space-time trellis coded modulation (STTCM) coding arrangement for a transmitter using two transmit antennas, in accordance with an embodiment of this invention. As in the case of Fig. 1, the two antennas are referenced 16 and 18, and input bits of information to be communicated are supplied to the S-P converter 10, which is again illustrated with two outputs for QPSK symbol transmission. The remainder of Fig. 4 represents the turbo STTCM coding arrangement, which comprises two RSC coder and mapping functions 30 and 32, an interleaver 34, and a selector 36 having two outputs for the respective transmit paths to the two antennas 16 and 18. Dashed lines at the inputs to the RSC coder and mapping functions 30 and 32 indicate that these, and the interleaver 34, may have a different number of inputs for other than QPSK symbols, as described above.

The bits supplied in parallel from the S-P converter 10 are interleaved in groups (in this case, in pairs) by the interleaver 34. The non-interleaved bit pairs supplied to the function 30, and the interleaved bit pairs supplied to the function 32, are coded and mapped into QPSK symbols by these functions as described further below. Consequently, the function 30 produces at its two outputs QPSK symbols SS1 which represent systematic information corresponding to the input bits, and QPSK symbols PS1 which represent parity information produced by the recursive convolutional coding of the function

30. Similarly, the function 32 produces at its two outputs QPSK symbols SS2 which represent systematic information corresponding to the input bits as interleaved in bit pairs by the interleaver 34, and QPSK symbols PS2 which represent parity information produced by the recursive convolutional coding of the function 32 from the interleaved input bit pairs. Although it is assumed here for convenience and simplicity that the RSC coding and mapping functions 30 and 32 are identical, as is typically the case for the component coders of a turbo coder as described above with reference to Fig. 3, this need not necessarily be the case and these functions could instead differ from one another.

The selector 36 is controlled by a control signal of alternating ones and zeros (1010... as illustrated) at the symbol (bit pair) rate, and performs selection and puncturing functions as represented in Fig. 4 by switches within the selector 36. In a first state of the control signal, for example when the control signal is a binary 1, the switches of the selector 36 have the states illustrated in Fig. 4 in which the systematic symbol SS1 and the parity symbol PS1 from the RSC coder and mapping function 30 are supplied to the output paths to the transmit antennas 16 and 18 respectively, and the outputs SS2 and PS2 of the function 32 are not used. In a second state of the control signal, for example when the control signal is a binary 0, the switches of the selector 36 have their opposite states in which the systematic symbol SS2 and the parity symbol PS2 from the RSC coder and mapping function 32 are supplied to the output paths to the transmit antennas 18 and 16 respectively, and the outputs SS1 and PS1 of the function 30 are not used.

It can be appreciated that, with the selector 36 alternately selecting the non-interleaved systematic symbols SS1 and the interleaved systematic symbols SS2, in order to

ensure that all of the systematic information is transmitted it is necessary for the interleaver 34 to map even positions at its input to even positions at its output, and odd positions at its input to odd positions at its output (or, alternatively, even-to-odd and odd-to-even position mapping), as in the case of the Robertson et al. arrangement discussed above. The interleaver 34 is arranged to provide such mapping accordingly.

From the above description and from Fig. 4 it can be appreciated that the units 30, 32, 34, and 36 are arranged in the manner of a turbo coder, for which the functions 30 and 32 provide recursive convolutional coding as is desired for a turbo coder, and the selector 36 combines the selection and puncturing functions of a turbo coder with the functions of a space-time block coder for transmit diversity using the two antennas 16 and 18. The even-to-even and odd-to-odd (or even-to-odd and odd-to-even) position mapping by the interleaver 34 ensures that systematic symbols representing all of the input bits are transmitted over time (i.e. in each interleaving block), despite the puncturing that is applied to the systematic symbols SS1 and SS2 individually. Thus the units 30, 32, 34, and 36 provide the combined functions of turbo coding, recursive trellis coded modulation, and space-time coding.

It is necessary to determine desirable recursive trellis or convolutional codes, and hence forms of the functions 30 and 32, for use in the arrangement described above with reference to Fig. 4. The encoding process can be described in various ways, one of which, adopted below, is by coder state and output matrices.

For a coder having N states and supplied with input symbols with M possible values (e.g. in this description M=4 for the paired input bits for QPSK), a coder state matrix B is

an N by M matrix (N rows and M columns) whose elements B(i,j) determine the coder state for the next symbol, depending upon the current state represented by i, which is an integer from 0 to N-1, and the current input symbol represented by j, which is an integer from 0 to M-1. A coder output matrix C is also an N by M matrix whose elements C(i,j) determine the output symbol produced when, similarly, the current coder state and the current input symbol are represented by i and j respectively.

For a coder having T output paths for supplying a corresponding number of antennas, a further coder output matrix Z is defined which is also an N by M matrix, derived from the matrix C, with elements Z(i,j) where i and j are as defined above. Each element Z(i,j) consists of T Q-ary symbols which identify the signal supplied to the respective antennas, where Q is determined by the modulation type and for example Q=4 for QPSK. Thus each element consists of T Q-ary symbols $z_t(i,j)$ identifying the signal supplied to the antenna t, where t is an integer from 0 to T-1.

The encoding process is further described by a mapping function from the coder outputs to the signal point constellations used for transmission. For simplicity and convenience, throughout the following description this mapping function is assumed to be as described above with reference to Fig. 2, i.e. a Gray code mapping for QPSK symbols.

Although an encoding process can be fully described for implementation in the manner outlined above, this is not sufficient to classify a code. For the latter purpose, a convolutional code can be described by a coder state matrix equation:

$$\Phi_{i+1} = W\,\Phi_i \oplus G\,U_i$$

and a coder output matrix equation:

$$Z_i = H_\varphi\,\Phi_i \oplus H_u\,U_i$$

where Φ_i is an n-dimensioned binary vector of the current coder state and $n=\log_2(N)$, U_i is an m-dimensioned binary input vector and $m=\log_2(M)$, Z_i is a p-dimensioned binary output vector, and $p=\log_2(P)$ and $P=Q^T$, $\oplus$ represents modulo-2 addition (or, equivalently, an exclusive-or function), and G, W, H_φ, and H_u are respective gain or weighting factor binary matrices.

To assist in an understanding in this respect, Fig. 5 illustrates a general form of convolutional or trellis coder which corresponds to the last two equations above. Referring to Fig. 5, this coder comprises multipliers 40 to 43 which are supplied with the respective gain or weighting factors. Each input symbol U_i is supplied to the multipliers 40 and 43, and the current coder state Φ_i is supplied to the multipliers 41 and 42. The outputs of the multipliers 40 and 41 are combined in a modulo-2 adder 44 in accordance with the first of the two equations above, the output of which adder is delayed by one symbol interval D in a delay unit 46 to provide the next coder state. The outputs of the multipliers 42 and 43 are combined in a modulo-2 adder 45 in accordance with the second of the two equations above, the output of which adder is supplied to a mapping function 47 which performs the QPSK mapping as described above. Multiple paths for vectors of dimension m, n, and p are denoted for some paths in Fig. 5 in conventional manner by bars on these paths.

A convolutional or trellis code can be classified using the matrix W and a matrix $H=[H_\varphi\ H_u]$. In particular, if each row of the matrix W contains no more than one "1", then the code is non-recursive, otherwise the code is recursive. Also, if the matrix H_u has a column with a single non-zero element at the j-th row position and the elements of the j-th row of the matrix H_φ are all "0", the code contains a systematic component for the j-th bit of the input sequence.

As discussed above, the codes described in the publication by Tarokh et al. referred to above are non-recursive and accordingly are unsuitable for providing an efficient turbo coder arrangement as illustrated in Fig. 4. For small numbers of coder states, the elements of the gain matrices that provide the best codes can be determined by computer searching and simulation, but this becomes impractical for coders with a large number of (e.g. more than 8) coder states, and other methods must be adopted. The codes described below were determined by selecting a prototype binary recursive convolutional code for transmission via a single antenna, using this to construct a trellis for space-time coding using the desired number of antennas, and then modifying the result to improve it for QPSK. Other codes, including codes arrived at in other ways, may alternatively be used, and the following codes are provided only by way of example.

For a 4-state RSC coder and QPSK mapping function which can be used in the transmitter of Fig. 4, the matrices B, C, Z, W, G, H_φ and H_u can be as follows:

$$B=\begin{bmatrix}0&3&2&1\\2&1&0&3\\3&0&1&2\\1&2&3&0\end{bmatrix}\qquad C=\begin{bmatrix}0&7&13&10\\3&4&14&9\\2&5&15&8\\1&6&12&11\end{bmatrix}\qquad Z=\begin{bmatrix}00&13&31&22\\03&10&32&21\\02&11&33&20\\01&12&30&23\end{bmatrix}$$

$$W=\begin{bmatrix}0&1\\1&1\end{bmatrix}\qquad G=\begin{bmatrix}1&0\\1&1\end{bmatrix}\qquad H_\varphi=\begin{bmatrix}0&0\\0&0\\1&0\\1&1\end{bmatrix}\qquad H_u=\begin{bmatrix}1&1\\0&1\\1&1\\1&0\end{bmatrix}$$

An implementation of such a coder and its mapping functions, which can be used to form each of the functions 30 and 32 in the arrangement of Fig. 4, is illustrated in Fig. 6.

Referring to Fig. 6, the coder comprises modulo-2 adders 50 to 54, two delay elements 55 and 56 each providing a

delay of one symbol (bit pair) interval D, and two mapping functions 57 and 58 each of which provides Gray code mapping of two bits supplied to its inputs to a QPSK symbol at its output, as described above with reference to Fig. 2.

A pair of input bits, supplied from the S-P converter 10 in the case of the function 30 or from the interleaver 34 in the case of the function 32 as described above with reference to Fig. 4, is supplied to inputs of the coder of Fig. 6 in each symbol interval. These bits are supplied to inputs of the adder 50, the output of which adder, and a lower one (as illustrated) of the bit inputs to the coder, are supplied to the mapping function 57, which produces at its output a Gray code QPSK mapped systematic symbol which represents the input bit pair.

The upper one (as illustrated) of the bit inputs to the coder of Fig. 6 is also supplied to an input of each of the adders 51 to 54, and the lower bit input to the coder is also supplied to another input of each of the adders 52 and 53. The output of the adder 51 is supplied to the delay element 55, whose output is supplied to another input of each of the adders 52 to 54. The output of the adder 52 is supplied to the delay element 56, whose output is supplied to another input of each of the adders 51, 52, and 54. It can be seen that the arrangement of the adders 51 to 54 and delay elements 55 and 56 of Fig. 6 implements the coder matrices described above; for example, there are three feedback paths from the delay elements 55 and 56 to inputs of the adders 51 and 52 configured according to the three ones in the matrix W given above, the two delay elements providing the four states of the coder. The outputs of the adders 53 and 54 constitute the inputs to the mapping function 58, which accordingly produces at its output a Gray code QPSK mapped parity symbol in accordance with the code given by the above equations.

For an 8-state RSC coder and QPSK mapping function which can be used in the transmitter of Fig. 4, the matrices B, C, Z, W, G, H_φ and H_u can be as follows:

$$B=\begin{bmatrix}0&3&1&2\\7&4&6&5\\1&2&0&3\\6&5&7&4\\3&0&2&1\\4&7&5&6\\2&1&3&0\\5&6&4&7\end{bmatrix}\quad C=\begin{bmatrix}0&6&15&9\\1&7&14&8\\1&7&14&8\\0&6&15&9\\3&5&12&10\\2&4&13&11\\2&4&13&11\\3&5&12&10\end{bmatrix}\quad Z=\begin{bmatrix}00&12&33&21\\01&13&32&20\\01&13&32&20\\00&12&33&21\\03&11&30&22\\02&10&31&23\\02&10&31&23\\03&11&30&22\end{bmatrix}$$

$$W=\begin{bmatrix}1&1&1\\1&0&1\\1&0&0\end{bmatrix}\quad G=\begin{bmatrix}1&1\\1&0\\0&0\end{bmatrix}\quad H_\varphi=\begin{bmatrix}0&0&0\\0&0&0\\1&1&1\\0&0&1\end{bmatrix}\quad H_u=\begin{bmatrix}1&1\\0&1\\0&1\\1&1\end{bmatrix}$$

An implementation of such a coder and its mapping functions, which can be used to form each of the functions 30 and 32 in the arrangement of Fig. 4, is illustrated in Fig. 7. From a comparison of the equations given above for this 8-state coder and the circuit of Fig. 7 (in which there are three delay elements to provide the 8 states), it can be seen that this circuit implements the recursive systematic convolutional coding of these equations.

For a 16-state RSC coder and QPSK mapping function which can be used in the transmitter of Fig. 4, the matrices B, C, Z, W, G, H_φ and H_u can be as follows:

$$B=\begin{bmatrix} 0 & 3 & 1 & 2 \\ 7 & 4 & 6 & 5 \\ 8 & 11 & 9 & 10 \\ 15 & 12 & 14 & 13 \\ 1 & 2 & 0 & 3 \\ 6 & 5 & 7 & 4 \\ 9 & 10 & 8 & 11 \\ 14 & 13 & 15 & 12 \\ 3 & 0 & 2 & 1 \\ 4 & 7 & 5 & 6 \\ 11 & 8 & 10 & 9 \\ 12 & 15 & 13 & 14 \\ 2 & 1 & 3 & 0 \\ 5 & 6 & 4 & 7 \\ 10 & 9 & 11 & 8 \\ 13 & 14 & 12 & 15 \end{bmatrix} \quad C=\begin{bmatrix} 0 & 7 & 10 & 13 \\ 3 & 4 & 9 & 14 \\ 2 & 5 & 8 & 15 \\ 1 & 6 & 11 & 12 \\ 1 & 6 & 11 & 12 \\ 2 & 5 & 8 & 15 \\ 3 & 4 & 9 & 14 \\ 0 & 7 & 10 & 13 \\ 2 & 5 & 8 & 15 \\ 1 & 6 & 11 & 12 \\ 0 & 7 & 10 & 13 \\ 3 & 4 & 9 & 14 \\ 3 & 4 & 9 & 14 \\ 0 & 7 & 10 & 13 \\ 1 & 6 & 11 & 12 \\ 2 & 5 & 8 & 15 \end{bmatrix} \quad Z=\begin{bmatrix} 00 & 13 & 22 & 31 \\ 03 & 10 & 21 & 32 \\ 02 & 11 & 20 & 33 \\ 01 & 12 & 23 & 30 \\ 01 & 12 & 23 & 30 \\ 02 & 11 & 20 & 33 \\ 03 & 10 & 21 & 32 \\ 00 & 13 & 22 & 31 \\ 02 & 11 & 20 & 33 \\ 01 & 12 & 23 & 30 \\ 00 & 13 & 22 & 31 \\ 03 & 10 & 21 & 32 \\ 03 & 10 & 21 & 32 \\ 00 & 13 & 22 & 31 \\ 01 & 12 & 23 & 30 \\ 02 & 11 & 20 & 33 \end{bmatrix}$$

$$W=\begin{bmatrix} 1 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \quad G=\begin{bmatrix} 1 & 1 \\ 1 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad H_\varphi=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 \end{bmatrix} \quad H_u=\begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{bmatrix}$$

An implementation of such a coder and its mapping functions, which can be used to form each of the functions 30 and 32 in the arrangement of Fig. 4, is illustrated in Fig. 8. From a comparison of the equations given above for this 16-state coder and the circuit of Fig. 8 (in which there are four delay elements to provide the 16 states), it can be seen that this circuit implements the recursive systematic convolutional coding of these equations.

It can be appreciated from the above description of the coding arrangement of Fig. 4 and the encoders of Figs. 6 to 8 that in each case, for QPSK symbols as described, there are two input bits in one symbol interval, resulting in four bits (two systematic information bits and two parity bits) being supplied to the QPSK mapping functions of each of the two coders in the turbo coding arrangement. These eight bits are

mapped into four QPSK symbols by the mapping functions, and over two successive symbol intervals half of the QPSK symbols are punctured by the selector 36 so that two symbols are transmitted from the two antennas 16 and 18 in each symbol interval. The selector arrangement is such that in a first symbol interval the two antennas transmit systematic and parity information from the coder 30 supplied with non-interleaved input bits, and in a second symbol interval the two antennas transmit systematic and parity information from the other coder 32 supplied with interleaved input bits, space-time diversity being enhanced by the transmission from each antenna of systematic information and parity information symbols alternately in successive symbol intervals.

In the arrangements described above, the mapping functions are arranged so that each QPSK symbol is produced entirely from systematic information or entirely from parity bits. However, this need not be the case, and alternative arrangements are possible in which, for example, each QPSK symbol is instead produced from one systematic information bit and one parity bit. In other words, the inputs to the mapping functions (e.g. 56 and 57 in Fig. 6) for each coder can be rearranged.

This is the case for the coder described by way of example below with reference to Fig. 9, for use in a turbo STTCM coding arrangement for use in a transmitter having four transmit antennas. By way of example, this is a 4-state trellis coder for QPSK symbols. In two successive symbol intervals for space-time diversity a total of eight symbols are transmitted from the four antennas, so that with 50% puncturing there are eight QPSK symbols provided by the mapping functions of the two component coders of the turbo coder arrangement, and consequently in each symbol interval each coder provides four QPSK symbols from its mapping functions. These four QPSK

symbols represent four systematic bits and four parity bits, so that in this case there are four input bit lines to the coder.

Referring to Fig. 9, the four input bit lines, collectively referenced 60, are connected each to a first input of four QPSK mapping functions 61 to 64 which provide Gray code mapping to QPSK symbols as described above with reference to Fig. 2. The coder also comprises two delay elements 65 and 66 each providing a delay D of one symbol interval, thereby determining the four states of the coder, and modulo-2 adders 67 to 72. The outputs of the modulo-2 adders 69 to 72 are connected each to a second input of the mapping functions 61 to 64, respectively. Thus the QPSK mapping functions 61 to 64 are each supplied with one systematic information bit and one parity bit, and produce QPSK symbols SP-1 to SP-4 respectively which combine this systematic and parity information.

The lines 60, delay elements 65 and 66, and modulo-2 adders 67 to 72 are otherwise interconnected as illustrated in Fig. 9 in a manner which implements the following matrices W, G, H_φ and H_u. In this example the matrices B, C, and Z are not provided because of their large size (for example, Z is a 4 by 64 matrix), but these can be derived from the illustration in Fig. 9 or from the following matrices:

$$W=\begin{bmatrix}1 & 0\\1 & 0\end{bmatrix} \qquad G=\begin{bmatrix}1 & 1 & 0 & 1\\0 & 1 & 1 & 0\end{bmatrix} \qquad H_\varphi=\begin{bmatrix}0 & 0\\1 & 0\\0 & 0\\0 & 1\\0 & 0\\1 & 1\\0 & 0\\1 & 0\end{bmatrix} \qquad H_u=\begin{bmatrix}1 & 0 & 0 & 0\\1 & 1 & 1 & 0\\0 & 1 & 0 & 0\\0 & 0 & 1 & 1\\0 & 0 & 1 & 0\\0 & 0 & 0 & 1\\0 & 0 & 0 & 1\\0 & 0 & 0 & 1\end{bmatrix}$$

Again, it should be appreciated that the connections to the mapping functions 61 to 64 in Fig. 9 are provided by way of example and can be rearranged for other codes and other

circumstances. For example, the four systematic bits could instead be supplied to two of the mapping functions, and the four parity bits could be supplied to the remaining two mapping functions. As another example, one of the mapping functions could be supplied with two systematic bits, another with two parity bits, and the remaining two each with one systematic and one parity bit. However, the particular arrangement of Fig. 9 is assumed for the further description below.

Fig. 10 illustrates parts of a turbo STTCM coding arrangement for a transmitter having four transmit antennas, in which the coder of Fig. 9 is used to constitute each of the two component coder and mapping function units 80 and 82 of the turbo coding arrangement. An S-P converter 84 is supplied with input bits and converts these into groups of four bits, which are supplied directly as the input bits of the unit 80 and via an interleaver 86 to the unit 82. The interleaver 86 interleaves groups of four bits, maintaining an even-to-even and odd-to-odd, or an even-to-odd and odd-to-even, position mapping as described above. The systematic and parity symbol outputs of the unit 80, collectively referenced SP1, are coupled to a first set of inputs of a selector 88, and the systematic and parity symbol outputs of the unit 82, collectively referenced SP2, are coupled via an optional phase rotation unit 90 to a second set of inputs of the selector 88. The selector 88 is controlled by an alternating sequence of one and zero bits to couple its first and second sets of inputs alternately in successive symbol intervals to four output paths to the four antennas, referenced 92.

The optional phase rotation unit 90 provides a phase rotation of each symbol by $\pi/2$, and can comprise four multipliers each arranged to multiply a respective one of the QPSK symbols supplied to it by a signal $e^{j\pi/2}$, this having been found to improve performance in some situations, in particular

in a transmitter using four antennas. This phase rotation unit can be omitted, a similar phase rotation unit can if desired be provided in a coding arrangement for a transmitter using only two antennas as described above, and/or phase rotations can be provided for some but not all of the QPSK symbols.

Thus it can be seen that the selector 88 couples to its outputs the systematic and parity information QPSK symbols from the unit 80 supplied with non-interleaved input bits in a first one of each two successive symbol intervals, and couples to its outputs the systematic and parity information QPSK symbols from the unit 82 supplied with interleaved input bits in a second one of each two successive symbol intervals.

Fig. 11 illustrates parts of a receiver and decoding arrangement for use with the arrangement of Fig. 4 or Fig. 10. As illustrated in Fig. 11, the receiver comprises two antennas 100 and 101 signals from which are coupled to and combined in a maximum ratio combiner (MRC) 102 to produce at its output on a line 103 a signal for decoding. For simplicity other known parts of the receiver, such as down converters and signal amplifiers and samplers, are not shown in Fig. 11 but are represented by dashed lines in the paths from the antennas 100 and 101 to the MRC 102. Although Fig. 11 illustrates the receiver as having two antennas, it may alternatively have only one antenna or more than two antennas, and methods other than maximum ratio combining may be used to produce the signal for decoding on the line 103.

The decoding arrangement comprises a de-puncturing selector 104, two soft trellis code decoders 105 and 106, an interleaver 107 which operates in the same manner as the interleaver of the turbo coding arrangement in the transmitter, e.g. the interleaver 34 in the arrangement of Fig. 4, and a de-interleaver 108 which operates in the converse manner to the

interleaver 107. The units 105 to 108 are arranged in a manner generally known in the art of turbo code decoders, with the first decoder 105 producing a soft output (probability vector) that is interleaved by the interleaver 107 and supplied as a soft input to the second decoder 106, which also produces a soft output which is de-interleaved by the de-interleaver 108 and supplied as a soft input to the first decoder in an iterative arrangement, with the first decoder 105 operating on a non-interleaved input vector and the second decoder 106 operating on an interleaved input vector, the input vectors being derived from the signal to be decoded on the line 103. After a desired number of iterations, an output is derived from the decoding arrangement, for example from the output of the de-interleaver 108 as illustrated in Fig. 11.

It will be recalled from the description above that the coding arrangement of Fig. 4 or Fig. 10 provides symbols derived from non-interleaved bits and symbols derived from interleaved input bits alternately in successive symbol intervals. Correspondingly, the selector 104 is controlled, by a control signal of alternating ones and zeros as illustrated in Fig. 11, to have each of two states alternately in successive symbol intervals. In a first one of these two states, in which the selector is represented by switches having the states as shown in Fig. 11 and corresponding to the transmission of symbols derived from non-interleaved input bits, the selector 104 supplies the signal on the line 103 as the input vector to the first decoder 105 and supplies a zero input vector to the second decoder 106. Conversely, in a second one of these two states, in which the selector is represented by switches having the states opposite to those shown in Fig. 11 and corresponding to the transmission of symbols derived from interleaved input bits, the selector 104 supplies a zero input vector to the first decoder 105 and

supplies the signal on the line 103 as the input vector to the second decoder 106. Thus the first decoder 105 operates on non-interleaved data, and the second decoder 106 operates on interleaved data, as is desired. The complexity of the decoders is simplified by the supply of the zero input vectors to these decoders in the alternating symbol intervals.

The performance of a coding and decoding arrangement as described above in accordance with an embodiment of this invention can usefully be compared with that of a concatenated turbo-TCM and STBC arrangement known from the prior art (Bauch) referred to in the Background of the Invention. In each case with two transmit antennas, two receive antennas, an interleaver block length of 1000 bits (500 symbols), and a Doppler frequency of 256 Hz, arrangements in accordance with the invention as described above have been found to provide a significant improvement, compared with the Bauch concatenated arrangement, in terms of bit error rate of about 0.75 to 1.1 dB over a range of signal (energy per information bit) to noise ratios from 1 to 4 dB.

Although particular embodiments of the invention are described in detail above, it can be appreciated that numerous modifications, variations, and adaptations may be made within the scope of the invention as defined in the claims.

WHAT IS CLAIMED IS:

1. A method of providing space-time diversity for information to be transmitted from a plurality T of antennas, comprising the steps of:

in each of a plurality of successive symbol intervals, producing T symbols comprising systematic information and parity information at outputs of each of two recursive systematic convolutional coders, to one of which coders input bits are supplied directly and to the other of which coders said information bits are supplied after interleaving of bit groups for respective symbol intervals in an interleaving block; and

selecting first and second different mappings, each of T symbols from said symbols produced at the outputs of the coders, in respective alternating symbol intervals for supply to the T antennas to provide said space-time diversity, the interleaving and mappings being arranged so that systematic information is selected for all of the input bits in the interleaving block.

2. A method as claimed in claim 1 wherein the first mapping selects the T symbols from one of the coders and the second mapping selects the T symbols from the other of the coders.

3. A method as claimed in claim 2 wherein T=2 and in each symbol interval each coder produces a systematic information symbol and a parity information symbol, wherein the first mapping provides the systematic information symbol and the parity information symbol from one of the coders for supply respectively to first and second antennas, and the second mapping provides the systematic information symbol and the parity information symbol from the other of the coders for supply respectively to the second and the first antennas.

4. A method as claimed in claim 1 or 2 wherein T is even and in each symbol interval each coder produces T/2 systematic information symbols and T/2 parity information symbols.

5. A method as claimed in claim 1 or 2 wherein the T symbols produced by each coder in each symbol interval include at least one symbol comprising systematic and parity information.

6. A method as claimed in claim 1, 2, 4, or 5 wherein T=2.

7. A method as claimed in claim 1, 2, 4, or 5 wherein T=4.

8. A method as claimed in any of claims 1 to 7 and including the step of changing a phase of symbols from the two coders relative to one another.

9. A method as claimed in any of claims 1 to 8 wherein the interleaved bit groups each comprise m bits where m is an integer, and symbols produced at the outputs of the coders comprise M-PSK symbols where $M=2^m$.

10. A coding arrangement comprising:

first and second recursive systematic convolutional coders each arranged to produce a plurality of T symbols in each of a plurality of successive symbol intervals from m bits supplied thereto, where m is an integer;

an interleaver arranged to interleave groups each of m input bits within an interleaving block with a mapping of even-to-even and odd-to-odd, or even-to-odd and odd-to-even, positions;

input bits supplied to the first coder and to the interleaver, and interleaved bits supplied from the interleaver to the second coder; and

a selector arranged to supply different ones of the T

symbols from the coders in alternate symbol intervals to respective ones of T output paths, the T symbols selected in each of the alternating symbol intervals including all of the systematic information from a respective one of the coders.

11. A coding arrangement as claimed in claim 10 wherein each coder produces M-PSK symbols where $M=2^m$.

12. A coding arrangement as claimed in claim 10 or 11 wherein T is even and in each symbol interval each coder produces T/2 systematic information symbols and T/2 parity information symbols, and the selector is arranged to supply each output path with a systematic information symbol and a parity information symbol alternately in successive symbol intervals.

13. A coding arrangement as claimed in claim 10 or 11 wherein in each symbol interval each coder produces at least one symbol comprising systematic information and parity information.

14. A coding arrangement as claimed in any of claims 10 to 13 wherein T=2.

15. A coding arrangement as claimed in any of claims 10 to 13 wherein T=4.

16. A coding arrangement as claimed in any of claims 10 to 15 and including a phase rotator for providing a $\pi/2$ phase rotation of symbols produced by one of the two coders.

17. A decoding arrangement for iteratively decoding received symbols coded by the coding arrangement of claim 10, comprising:

first and second soft output decoders for decoding the coding by said first and second recursive systematic convolutional coders respectively, in response to an input

vector and soft input information;

an interleaver corresponding to the interleaver of the coder, arranged to couple soft output information from the first decoder as soft input information to the second decoder;

a de-interleaver converse to said interleavers, arranged to couple soft output information from the second decoder as soft input information to the first decoder; and

a selector arranged to supply a received signal vector and a zero input vector alternately in successive symbol intervals as the input vector to the first and second decoders.

18. A method of iteratively decoding a received signal comprising symbols coded by the method of claim 1, comprising the steps of:

supplying a received signal vector and a zero input vector alternately in successive symbol intervals as input vectors to two decoders for decoding the coding by said two recursive systematic convolutional coders respectively;

interleaving, in the same manner as in the method of coding, a soft output of one of the decoders, corresponding to said one of the coders, to provide a soft input to the other of the decoders; and

de-interleaving, conversely to the interleaving, a soft output of said other of the decoders to provide a soft input to said one of the decoders.

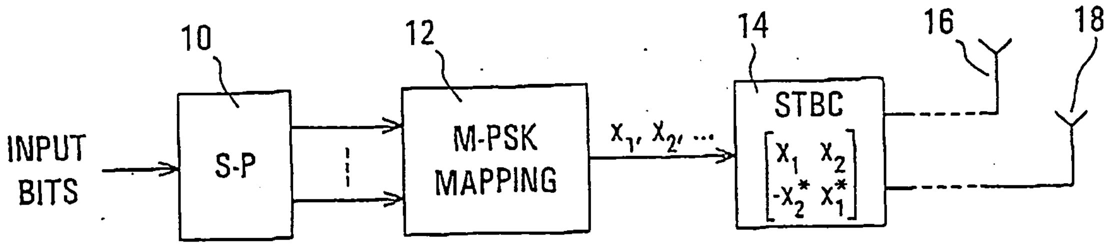


FIG. 1 PRIOR ART

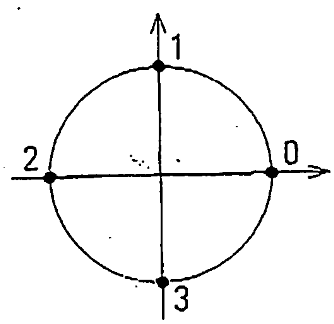


FIG. 2 PRIOR ART

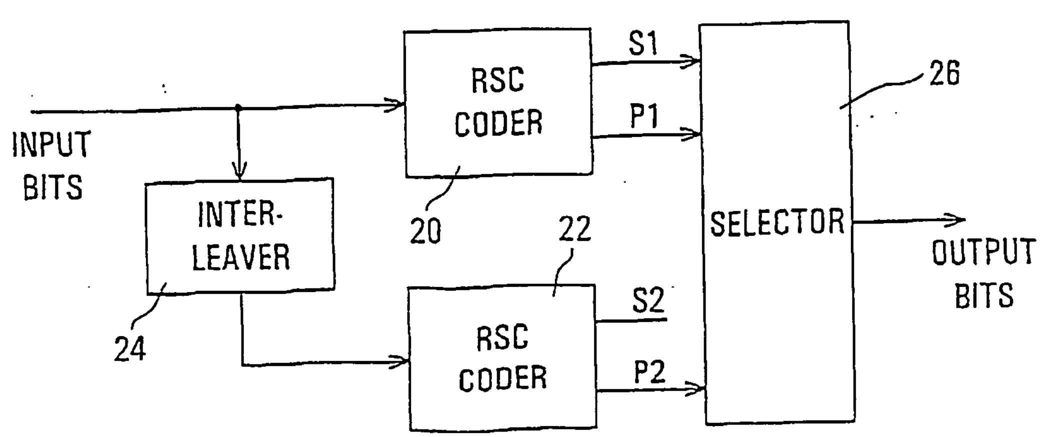


FIG. 3 PRIOR ART

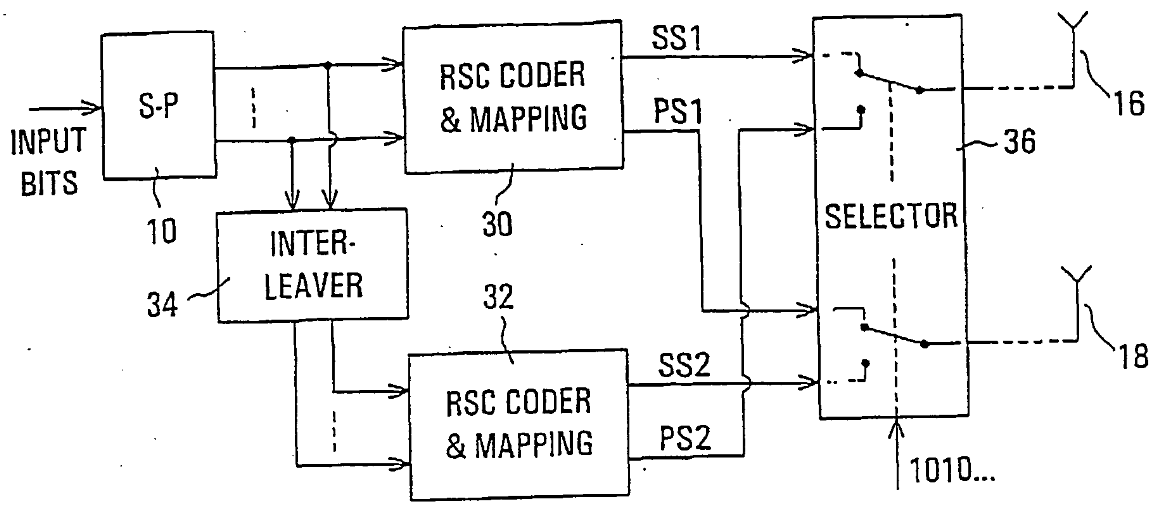

INPUT BITS
S-P
10
RSC CODER & MAPPING
30
INTER-LEAVER
34
32
RSC CODER & MAPPING
SS1
PS1
SS2
PS2
SELECTOR
36
16
18
1010...

FIG. 4

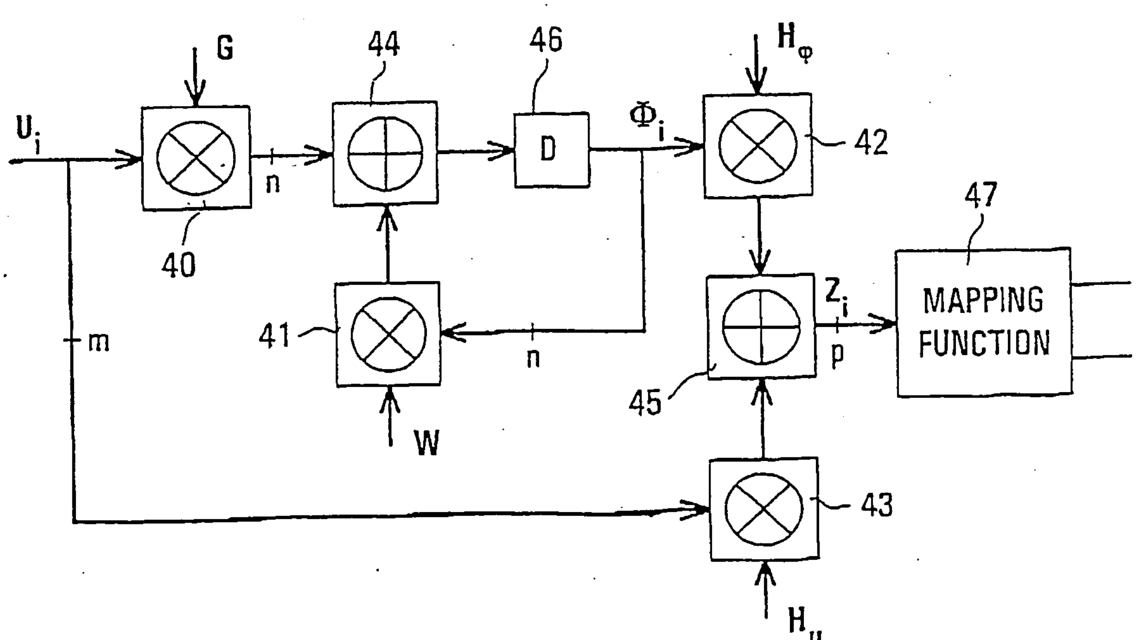

G
44
46
D
Hφ
Ui
Φi
42
n
40
41
m
n
W
47
Zi
p
MAPPING FUNCTION
45
43
Hu

FIG. 5

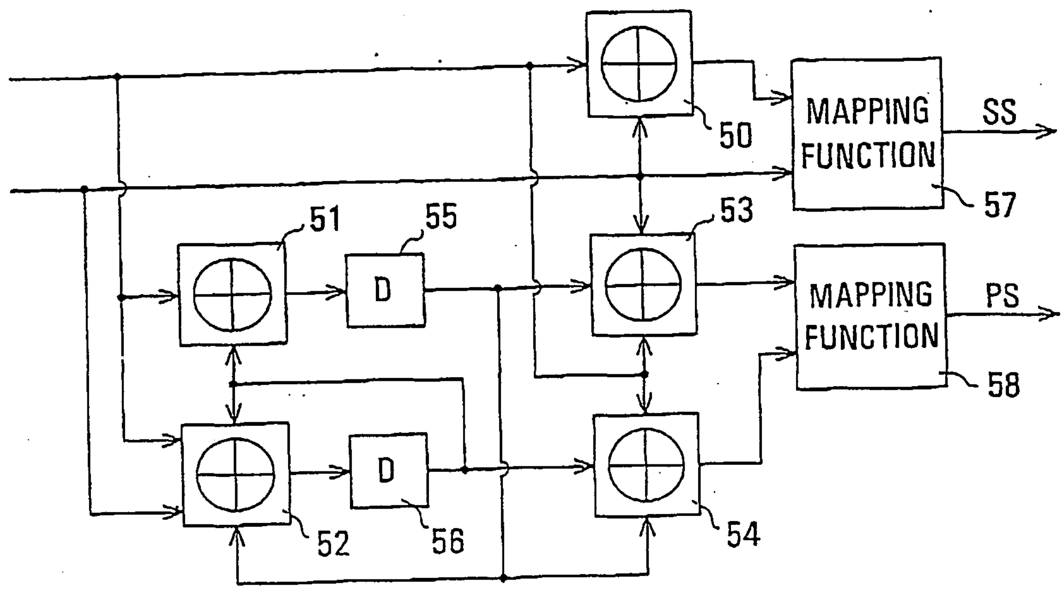

MAPPING FUNCTION
SS
MAPPING FUNCTION
PS
D
D
50
51
52
53
54
55
56
57
58

FIG. 6

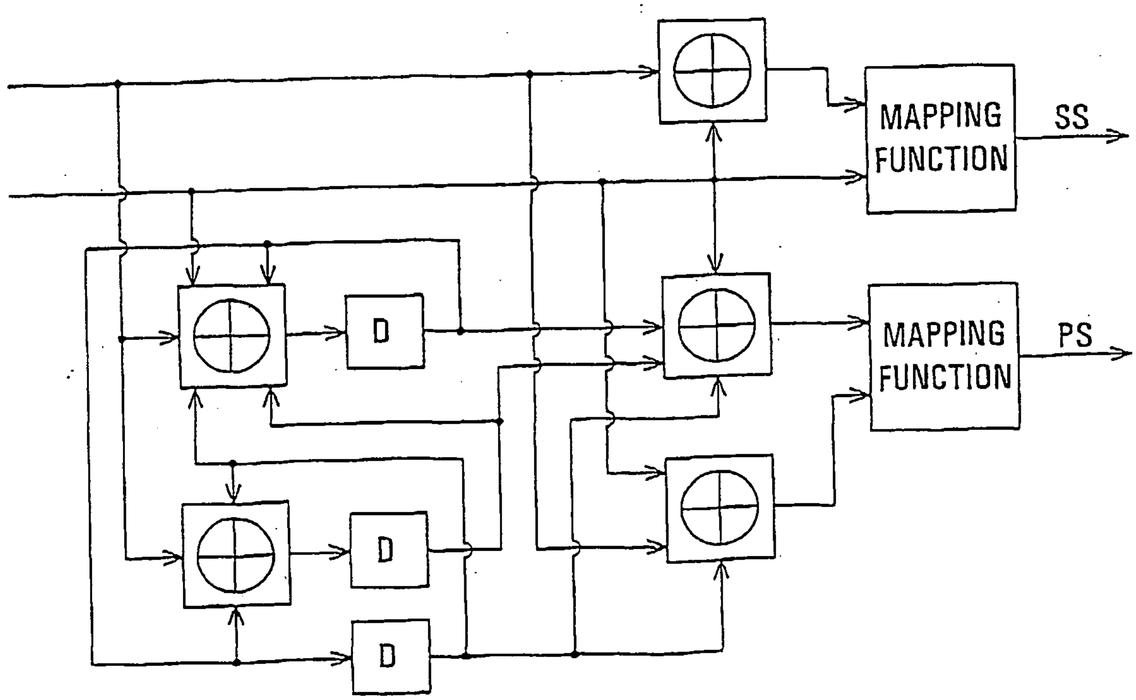

MAPPING FUNCTION
SS
MAPPING FUNCTION
PS
D
D
D

FIG. 7

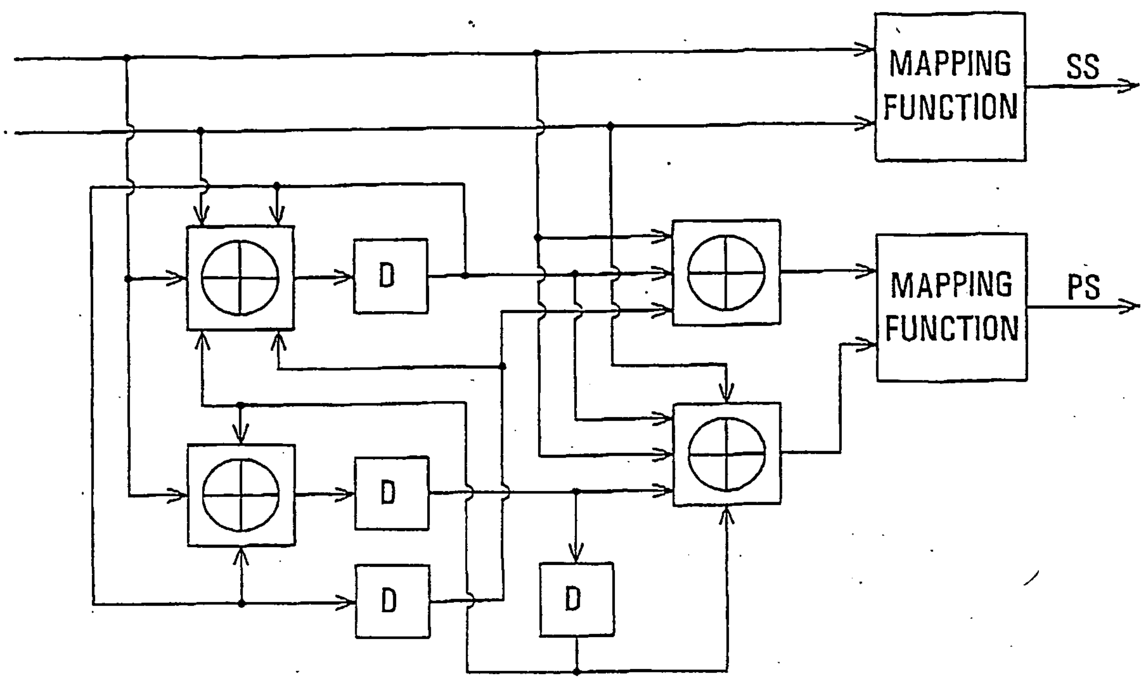

MAPPING FUNCTION
SS
MAPPING FUNCTION
PS
D
D
D
D

FIG. 8

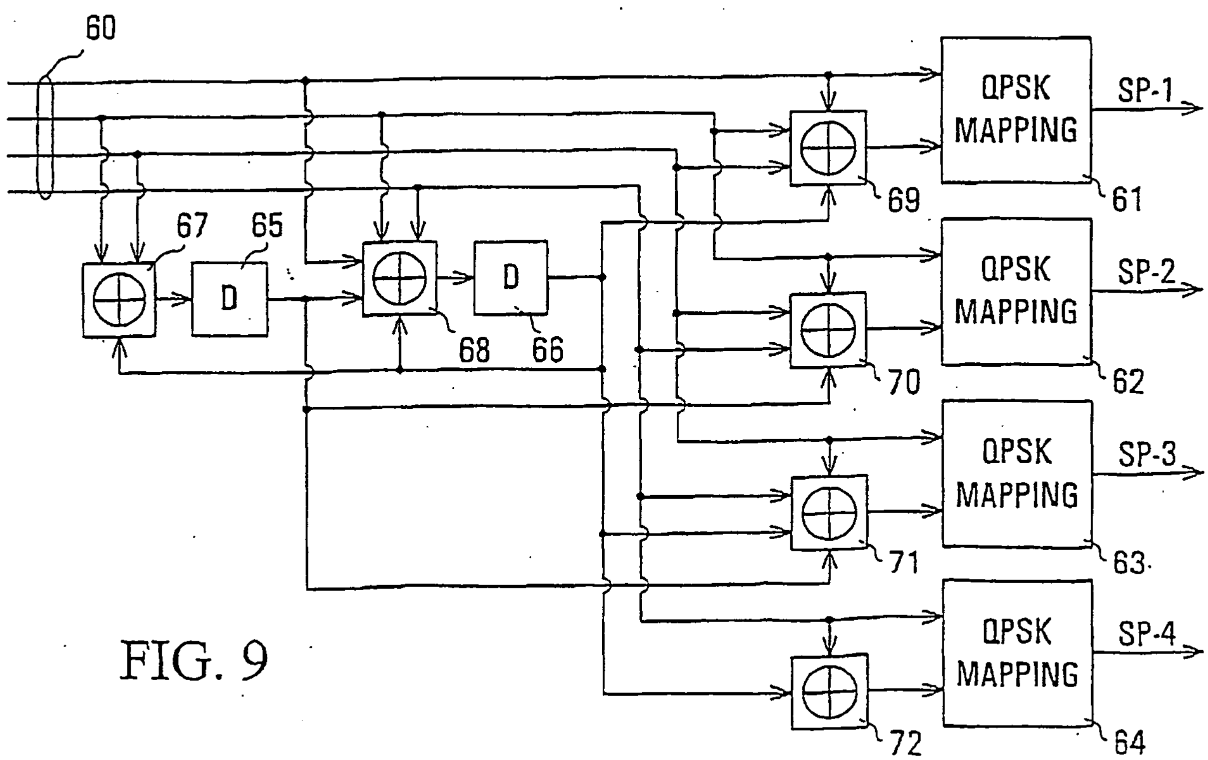

60
67
65
D
D
68
66
QPSK MAPPING
SP-1
61
69
QPSK MAPPING
SP-2
62
70
QPSK MAPPING
SP-3
63
71
QPSK MAPPING
SP-4
64
72

FIG. 9

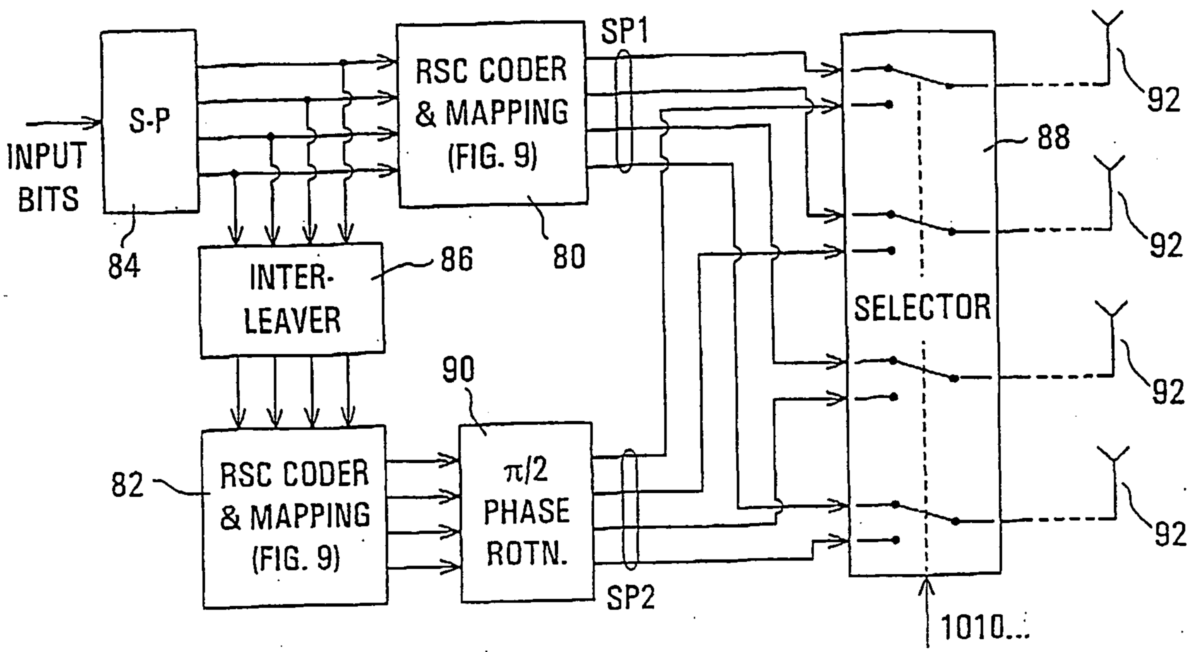

INPUT BITS
S-P
84
RSC CODER & MAPPING (FIG. 9)
80
SP1
INTER-LEAVER
86
RSC CODER & MAPPING (FIG. 9)
82
90
π/2 PHASE ROTN.
SP2
SELECTOR
88
92
92
92
92
1010...

FIG. 10

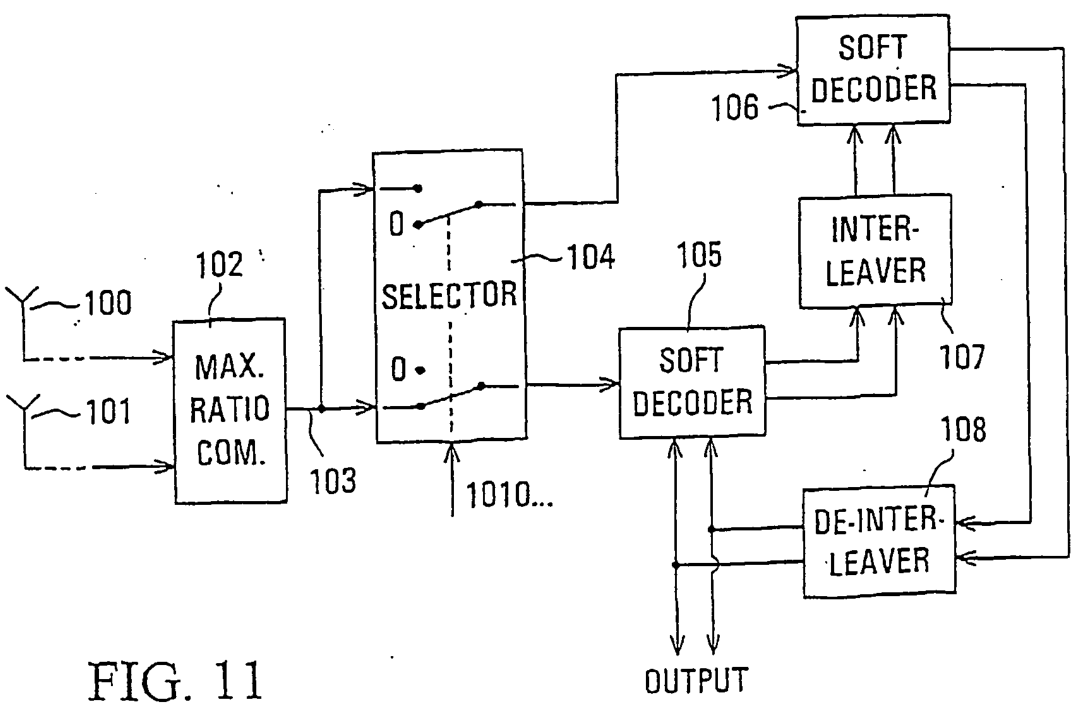

100
101
102
MAX. RATIO COM.
103
SELECTOR
0
0
104
1010...
105
SOFT DECODER
106
SOFT DECODER
INTER-LEAVER
107
108
DE-INTER-LEAVER
OUTPUT

FIG. 11

INTERNATIONAL SEARCH REPORT

Inter Application No
PCT/RU 00/00475

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L1/00 H04L1/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	YAMASHITA M ET AL: "Transmit diversity technique using space division multiplexing and turbo codes" ELECTRONICS LETTERS, 1 FEB. 2001, IEE, UK, vol. 37, no. 3, pages 184-185, XP002176430 ISSN: 0013-5194 right-hand column, line 19 - line 36; figure 1	1-6,9-14
A		17,18

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[X] Further documents are listed in the continuation of box C.

[ ] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 August 2001	12/09/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Papantoniou, A

INTERNATIONAL SEARCH REPORT

Int. Application No
PCT/RU 00/00475

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BAUCH G: "CONCATENATION OF SPACE-TIME BLOCK CODES AND ''TURBO''-TCM" ICC '99. 1999 IEEE INTERNATIONAL CONFERENCE ON COMMUNICATIONS. CONFERENCE RECORD. VANCOUVER, CA, JUNE 6 - 10, 1999, IEEE INTERNATIONAL CONFERENCE ON COMMUNICATIONS, NEW YORK, NY: IEEE, US, vol. 2, 6 June 1999 (1999-06-06), pages 1202-1206, XP000898047 ISBN: 0-7803-5285-8	17,18
A	page 1204, right-hand column, line 1 - line 11; figures 4,5 page 1204, right-hand column, line 15 - line 30 ---	1,10
X	ROBERTSON P ET AL: "BANDWIDTH-EFFICIENT TURBO TRELLIS-CODED MODULATION USING PUNCTURED COMPONENT CODES" IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, IEEE INC. NEW YORK, US, vol. 16, no. 2, 1 February 1998 (1998-02-01), pages 206-218, XP000741775 ISSN: 0733-8716	17,18
A	page 207, right-hand column, line 1 - line 3; figures 4,5 page 207, right-hand column, line 24 - line 28 page 208, right-hand column, line 6 - line 10 page 211, right-hand column, paragraph 2 ---	1,10
A	TUJKOVIC D: "Recursive space-time trellis codes for turbo coded modulation" GLOBECOM '00 - IEEE. GLOBAL TELECOMMUNICATIONS CONFERENCE. CONFERENCE RECORD (CAT. NO.00CH37137), PROCEEDINGS OF GLOBAL TELECOMMUNICATIONS CONFERENCE, SAN FRANCISCO, CA, USA, 27 NOV.-1 DEC. 2000, pages 1010-1015 vol.2, XP002176431 2000, Piscataway, NJ, USA, IEEE, USA ISBN: 0-7803-6451-1 page 1011, right-hand column, paragraph 2 - paragraph 3; figure 2 -----	1,10,17, 18